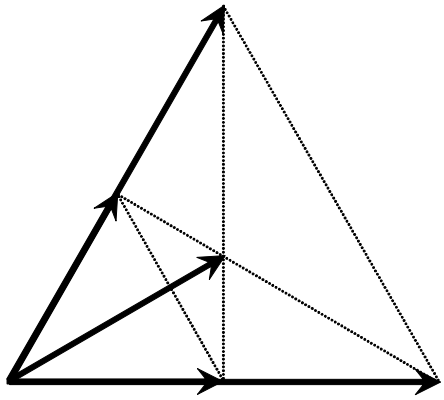
UNIVERSITAT POLITÈCNICA DE CATALUNYA

DEPARTAMENT D'ENGINYERIA ELECTRÒNICA

TESIS DOCTORAL

A Novel Pulsewidth Modulation for the Comprehensive Neutral-Point Voltage Control in the Three-Level Three-Phase Neutral-Point-Clamped Dc-Ac Converter



Sergio Busquets Monge

Octubre 2005

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Memoria presentada por

Sergio Busquets Monge

para acceder al grado de

Doctor en Ingeniería Industrial

Director: Dr. Josep Bordonau Farrerons

Barcelona, octubre 2005

A mi familia y amigos

Who dares to look for order in the land of nonsense?

Only a fool would do so. And it turns out that the one writing these lines once decided he wanted to be a fool. The willingness to lose one's mind is not in our nature. One is usually pushed by a number of factors. In my case, these factors have first and last names. There is a number of people I should mention here, since many are to blame for my incipient madness: starting with my parents and family, and following with my school and university friends, my friends from CPES, Crown Intl., and GREP… The list is too long and I would definitely forget some. And since this would be unfair for those declared guilty here, I have decided to forgive them all. Well, all but two people, the two most responsible of fooling me; i.e., the two most responsible of pushing me into the dark dimension of Power Electronics, trying to look for something that supposedly is there but nobody has seen it before. I am talking about Dr. Josep Bordonau, who subtly introduced me into the world of research and Power Electronics, and Dr. Dushan Boroyevich, who brought me deep into the dark, led by his light, and left me there. Yes, they deserve no mercy!

I would like to specially express my gratitude to Gerald R. Stanley, for his patient teaching during my times at Crown, and to Dr. Frank Munuera, for his invaluable support through critical moments in my life.

Do not expect to find wisdom in the following pages, but the first attempts of a fool's apprentice to find order in the land of nonsense.

CONTENTS

ABSTRACT

Multilevel converter topologies have received special attention during the last two decades due to their significant advantages in high-power medium- and high-voltage applications. In these topologies, and compared to the previous two-level case, the voltage across each semiconductor is reduced, avoiding the problems of the series interconnection of devices. The harmonic distortion of the output voltage is also diminished and the converter efficiency increases. But a larger number of semiconductors is needed and the modulation strategy to control them becomes more complex.

Among these topologies, the three-level three-phase neutral-point-clamped voltage source inverter is probably the most popular. The application of traditional modulation techniques to this converter causes a low frequency (three times the fundamental frequency of the output voltage) oscillation of the neutral-point voltage. This, in turn, increases the voltage stress on the devices and generates low-order harmonics in the output voltage.

This thesis presents a novel pulsewidth modulation for the three-level three-phase neutral-point-clamped converter, able to achieve a complete control of the neutral-point voltage while also having a low output voltage distortion at around the switching frequency. The new modulation, based on a virtual space vector concept, guarantees the balancing of the neutral-point voltage for any load (linear or nonlinear, any load power factor) over the full range of converter output voltage, the only requirement being that the addition of the output three-phase currents equals zero.

The performance of this modulation approach and its benefits over other previously proposed solutions are verified through simulation and experiments in both open- and closed-loop converter configurations.

NOMENCLATURE

Acronyms and Abreviations

3L	Three level
3P	Three phase
NPC	Neutral-point clamped
VSI	Voltage source inverter
PWM	Pulsewidth modulation
SVD	Space vector diagram
NTV	Nearest-three space vectors
VV	Virtual space vector
NTV^2	Nearest-three virtual space vectors
$ONTV^2$	Optimized nearest-three virtual space vectors
IGBT	Insulated-gate bipolar transistor
GTO	Gate turn-off thyristor
FPGA	Field programmable gate array
FFT	Fast Fourier transform.

Symbols

Time and Frequency

t	Time
t_{sw}	Switching time
T_s	Switching period
f	Frequency

f_s	Switching frequency
f_o	Converter output-voltage fundamental frequency
ω	Angular frequency
ω_s	Switching angular frequency
ω_o	Converter output-voltage fundamental angular frequency.

Frames

a-b-c	Canonical three-dimensional axis set
α-β-γ	Orthogonal axis set with $\gamma \parallel (1,1,1)_{a\text{-}b\text{-}c}$ and $\beta \parallel$ [projection of axis b^{Δ} onto plane π]
d-q-0	Generic *d-q-0* frame (unspecified axis *d* alignment)
d_1-q_1-0_1	*d-q-0* frame where axis *d* is aligned with $\mathbf{V}_{ref}$
d_2-q_2-0_2	*d-q-0* frame where axis *d* is aligned with $\mathbf{V}_{L\text{-}N}$.

Devices

S_i ; i = 1, 2…6	Converter outer switches
S_{ii} ; i = 1, 2…6	Converter inner switches
D_i ; i = 1, 2…6	Converter outer diodes
D_{ii} ; i = 1, 2…6	Converter inner diodes
D_{ci} ; i = 1, 2…6	Converter clamping diodes
A_i ; i = 1, 2…6	Converter outer modules
B_i ; i = 1, 2, 3	Converter inner modules.

Passives

R_L	Load resistance
R_s	Switch on-state resistance
R_d	Diode on-state resistance
R_{xy} ; $x, y \in \{a, h, i, j\}$	Thermal resistance between nodes x and y
L_L	Load inductance
L_S	Source inductance: Inductance of the boost rectifier used to connect the ac mains/generator to the dc link
C_1, C_2	Upper and lower converter dc-link capacitances
C_{dc}	Capacitance value of each dc-link capacitor (case $C_1 = C_2$)
C_L	Load capacitance
C_{xy} ; $x, y \in \{a, h, i, j\}$	Thermal capacitance between nodes x and y.

Voltages

v_{pn}	Converter dc-link voltage
v_p, v_o, v_n	Nodes p, o, and n voltages with reference to an undefined node
v_{C1}, v_{C2}	Upper and lower dc-link capacitor voltages
v_{unb}	Dc-link capacitor voltage unbalance
v_{uv}, v_{vw}, v_{wu}	Line-to-line ac-mains/generator voltages
v_{ab}, v_{bc}, v_{ca}	Line-to-line converter output voltages
v_{aN}, v_{bN}, v_{cN}	Line-to-neutral converter output voltages
$v_{\alpha\beta}$, $v_{\beta\gamma}$, $v_{\gamma\alpha}$	Line-to-line voltages at the ac-side of the non-linear-load three-phase diode rectifier
v^r_{ab}	Ripple in voltage v_{ab}
$V_{ab,n,k}$, $V_{bc,n,k}$, $V_{ca,n,k}$; $n, k \in N$	Three-phase line-to-line voltage harmonic amplitude at frequency $n{\cdot}f_s$ for switching cycle k

$V_{aN,n,k}$, $V_{bN,n,k}$, $V_{cN,n,k}$; $n, k \in N$	Three-phase line-to-neutral voltage harmonic amplitude at frequency $n \cdot f_s$ for switching cycle k
V_h ; $h \in N$	Rms value of the h^{th} harmonic of the converter output voltage
$V_{dis,n}$; $n \in N$	Converter output-voltage distortion around $n \cdot f_s$
$V_{max,n}$; $n \in N$	Maximum harmonic amplitude of the converter output voltage around $n \cdot f_s$
v_d, v_q	d-q components of the converter output three-phase voltages
v_s	Switch collector-to-emitter voltage
V_s	Switch on-state constant forward voltage drop
V_d	Diode on-state constant forward voltage drop.

Currents

I	Dc current source value
i_o	Neutral-point current
i_u, i_v, i_w	Three-phase ac-mains/generator currents
i_a, i_b, i_c	Converter output three-phase currents
i_{d1}, i_{q1}	d_1-q_1 components of the converter output three-phase currents
i_{d2}, i_{q2}	d_2-q_2 components of the converter output three-phase currents
i_s	Switch collector current.

Power

p_{cond}	Conduction power loss
p_{sw}	Switching power loss
p_{loss}	Total power loss.

Temperatures

T_a	Ambient temperature
T_h	Heat-sink temperature
T_c	Case temperature
T_i	Temperature at the point of common coupling of different devices integrated together
T_j	Junction temperature
ΔT_j	Junction temperature variation.

Switching States, Vectors and Matrices

xyz ; $x, y, z \in \{p, o, n\}$	Switching state, where phase a is connected to x, phase b to y and phase c to z
$\mathbf{V}_{\text{L-N}}$	Mains line-to-neutral voltage space vector
$\mathbf{V}_{\text{ref}}$	Converter output reference voltage space vector
$\mathbf{VV}_i$; $i = 1, 2, 3$	i^{th} virtual voltage space vector
$\mathbf{V}_0$, $\mathbf{V}_{Si}$, $\mathbf{V}_{Mi}$, $\mathbf{V}_{Li}$; $i = 1, 2\ldots6$	Original zero, small, medium and large voltage space vectors
$\mathbf{V}_{Z0}$, $\mathbf{V}_{ZSi}$, $\mathbf{V}_{ZMi}$, $\mathbf{V}_{ZLi}$; $i = 1, 2\ldots6$	Zero, small, medium and large virtual voltage space vectors
$\mathbf{V}_{G0}$, $\mathbf{V}_{GSi}$, $\mathbf{V}_{GMi}$, $\mathbf{V}_{GLi}$; $i = 1, 2\ldots6$	Zero, small, medium and large general virtual voltage space vectors
$\mathbf{V}_{\text{app}}$	Applied voltage space vector
$\mathbf{V}_{ei}$; $i \in N$	i^{th} error vector within a switching cycle
$v_{e\alpha}$, $v_{e\beta}$	Projections in axis α and β of the sequence of error vectors within a switching cycle
$\mathbf{V}^{+}_{H\alpha n}$, $\mathbf{V}^{-}_{H\alpha n}$; $n \in N$	Positive and negative rotating vectors of order n corresponding to $v_{e\alpha}$

$\mathbf{V}^{+}_{H\beta n}$, $\mathbf{V}^{-}_{H\beta n}$; $n \in N$	Positive and negative rotating vectors of order n corresponding to $v_{e\beta}$
$\mathbf{V}^{+}_{Hn}$, $\mathbf{V}^{-}_{Hn}$; $n \in N$	Positive and negative rotating vectors of order n
$\mathbf{V}_{Hn}$; $n \in N$	Pulsating vector of order n
$\mathbf{V}_{H}$	Vector equivalent to the sequence of error vectors
$[T]$	a^{Y}-b^{Y}-c^{Y} to d_1-q_1-0_1 transformation matrix
v_{refd}, v_{refq}	d_2-q_2 components of $\mathbf{V}_{ref}$
m	Modulation index (length of $\mathbf{V}_{ref}$)
m_{bAB}	Modulation index corresponding to the boundary between regions A and B of the m - φ operating plane
m_{bBC}	Modulation index corresponding to the boundary between regions B and C of the m - φ operating plane
NF	Normalizing factor for voltages in the SVD

Duty Ratios

d_{V0}, d_{VSi}, d_{VMi}, d_{VLi}	Duty ratios of the original space vectors
d_{VZ0}, d_{VZSi}, d_{VZMi}, d_{VZLi}	Duty ratios of the virtual space vectors
d_{VVi}	Duty ratio of virtual space vector $\mathbf{VV}_i$
d_{xyz}	Duty ratio of switching state xyz
d_{xy} ; $x \in \{a, b, c\}$, $y \in \{p, n\}$	Phase duty-ratios: duty ratio of the phase x connection to dc-link point y
d_{xy} ; $x \in \{p, n\}$, $y \in \{d, q, 0\}$	Phase duty-ratios in d_1-q_1-0_1 coordinates
d_{offset}	Offset applied to the phase duty-ratios
d'_{xy} ; $x \in \{a, b, c\}$, $y \in \{p, n\}$	Modified phase duty-ratios (addition of d_{offset}).

Angles

θ	$\mathbf{V}_{ref}$ angle with reference to axis α
φ	Load line-to-neutral impedance angle
ψ	$\mathbf{V}_{L\text{-}N}$ angle with reference to axis α
ϕ	$\mathbf{V}_{ref}$ angle with reference to $\mathbf{V}_{L\text{-}N}$
δ	$\mathbf{V}_{Hn}$ angle with reference to axis α
α_1, α_2	Line-cycle angle intervals where both d_{ap} and d_{an} are different from zero.

Modulation Parameters

r_i ; i =1, 2…7	Coefficients of the linear combination of different space vectors to obtain the general virtual space vectors
K	Amplitude of the sinusoidal term defining d_{pq} in the ONTV^2 PWM
K_A, K_B, K_C	Value of K in regions A, B, and C of the m - φ operating plane.

Distortion Figures

HDF	Harmonic distortion factor
$HD_{n,k}$; $n, k \in N$	Harmonic distortion of order n per switching cycle k
HD_n ; $n \in N$	Harmonic distortion of order n
THD	Total harmonic distortion
a_n, b_n ; $n \in N$	General Fourier series coefficients of order n
$a_{\alpha,n}$, $a_{\beta,n}$; $n \in N$	Fourier series coefficients of order n of $v_{e\alpha}$ and $v_{e\beta}$
K_T	Total number of switching cycles within the 1st sextant of the SVD
Ei ; i =1, 2…9	Auxiliary expressions to compute the value of $a_{\alpha,n}$ and $a_{\beta,n}$ as a function of the 3L-3P NPC VSI switching state duty-ratios.

Control Functions and Signals

f_i, f_{ii} ; i = 1, 2…6	Static control functions
$H_o(s)$	v_{unb} compensator transfer function
$H_v(s)$	v_{pn} error compensator transfer function
$H_{id}(s)$	i_{d2} error compensator transfer function
$H_{iq}(s)$	i_{q2} error compensator transfer function
NLB	Non linear-and-balanced load flag.

Special Subscripts, Superscripts, and Operators

Subscript ‘opt’	Optimum value
Subscript ‘max’	Maximum value
Subscript ‘min’	Minimum value
Superscript ‘Δ’	Refers to line-to-line voltages
Superscript ‘Y’	Refers to line-to-neutral voltages
Superscript ‘*’	Command value
Superscript ‘av’	Average value over a line cycle
$\langle x \rangle$	Local average value of x over the switching period.

CHAPTER 1

INTRODUCTION

Abstract — This introductory chapter reviews the basics of multilevel conversion and, in particular, the state o the art in modulation strategies for the three-level three-phase neutral-point-clamped voltage source dc-ac converter. The thesis objective is then defined, and finally, the outline of the thesis is presented.

1.1. Multilevel Conversion

Multilevel converter technology [1], [2] has received special attention during the last two decades due to its significant advantages in high-power medium- and high-voltage applications. The idea is to utilize multiple voltage levels in the process of dc-ac power conversion. Fig. 1.1 presents a functional schematic of a dc-ac converter leg having different number of levels. Fig. 1.1(a) corresponds to the conventional two-level inverter, Fig. 1.1(b) corresponds to the three-level case, and Fig. 1.1(c) to an *n*-level dc-ac converter. The converters are classified according to the number of dc-link voltage levels available to synthesize the output phase voltage v_a.

The topologies used to implement such converters include an array of power semiconductors and capacitor voltage sources. Three main different topologies have been proposed for multilevel inverters: diode-clamped, capacitor-clamped and cascaded multicell with separate dc sources. Fig. 1.2(a) presents the diode-clamped former topology, the popular three-level (3L) three-phase (3P)

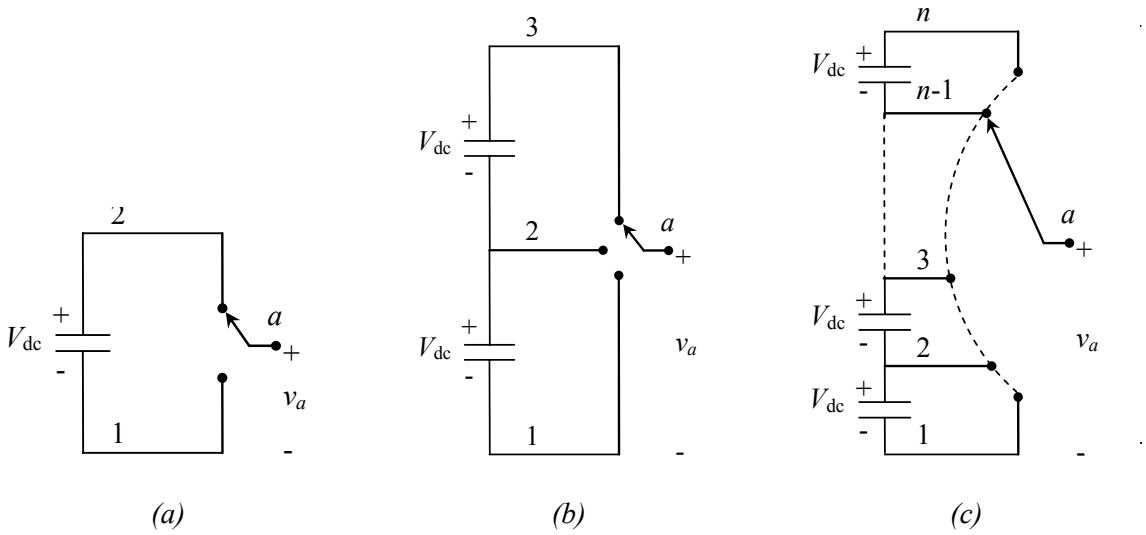
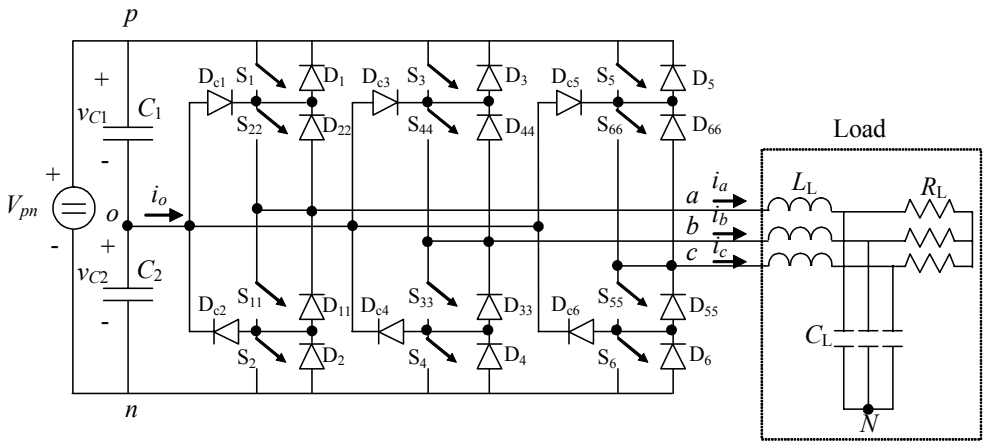
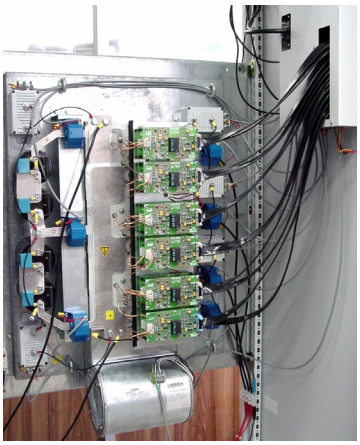


Fig. 1.1. Functional schematic of a dc-ac converter leg having different number of levels. (a) Two levels. (b) Three levels. (c) n levels.



(a)



(b)

Fig. 1.2. 3L-3P NPC VSI. (a) Schematic. (b) Prototype [100 kW, using 100 A/1200 V IGBTs SKM100)].

neutral-point-clamped (NPC) voltage source inverter (VSI), introduced by Nabae *et al*. [3].

Multilevel converters are used or currently under consideration in a number of different applications: large ac motor drives (for fans, pumps, blowers, compressors, conveyors, laminators, traction systems, paper and metal mill systems), utility interface applications such as static var compensators, active filters, high-voltage dc transmission systems, rectifiers for telecommunication equipment, unified power-flow controllers, dc-dc converters with high frequency isolation, distributed energy generation systems from renewable energy sources (wind generators, photovoltaic panels, fuel cells), and superconducting magnetic energy storage systems.

The main advantages of multilevel converters compared to the traditional two-level topology can be summarized as follows. For a desired operating dc-bus voltage, multilevel converters allow the use of semiconductor devices with a voltage rating lower than the dc-bus voltage (by a factor *n*-1) without the problems associated to the series connection of devices. We may need/prefer such

operating scheme either because the voltage rating of the available devices is lower than the desired dc-bus voltage or because we are interested in using specific devices with low cost and/or higher performance characteristics. Moreover, the output ac-voltage distortion is lower than in the two-level case, allowing for a reduction of the output filter passive components, which also leads to an improved dynamic response of the controlled converter. Last, the efficiency is also higher.

The use of multilevel topologies, however, requires a larger number of semiconductors and the modulation strategy to control them becomes more complex.

1.2. Three-Level Three-Phase NPC Dc-Ac Converter. State of the Art in Modulation Strategies.

The present thesis limits its scope to the most popular topology nowadays, the 3L-3P NPC converter in Fig. 1.2. It focuses on the use of this topology in applications allowing high switching-frequency (f_s) = ω_s / 2π) pulsewidth modulation (PWM).

There have been many studies with regard to the different possible modulations suitable for this converter [4]-[46]. The proposed modulations can be classified into two groups, according to their different implementation:

- Carrier-based modulations, where a modulating signal is compared to two triangular carrier waveforms.
- Space-vector-diagram (SVD) based modulations, where the modulation is defined from a vectorial representation of the available converter switching states.

In fact, as discussed in [34] and [44], for any carrier-based modulation there is an equivalent SVD-based modulation and vice versa. Therefore, in the following, the discussion of the different modulation proposals appearing in the literature will be presented, for simplicity, with reference to the converter SVD, shown in Fig. 1.3.

The vectors in the SVD of a multilevel three-phase converter are defined with three components, in a set of orthogonal axes a^{Δ}-b^{Δ}-c^{Δ} (Fig. 1.4), equal to the three line-to-line voltages corresponding to each converter switching state. Since the addition of the three line-to-line voltages equals zero, the vectors lie in plane π of Fig. 1.4, perpendicular to direction $\gamma = [1, 1, 1]_{a\text{-}b\text{-}c}$. Hence the SVD can be represented in two dimensions, corresponding to plane π. The same vector diagram results in a balanced system if properly scaled line-to-neutral voltages are assigned to axes a^{Y}-b^{Y}-c^{Y}, where this new set of axes is obtained rotating a^{Δ}-b^{Δ}-c^{Δ} 30º around γ (projection of a^{Y} on $\pi = \alpha$).

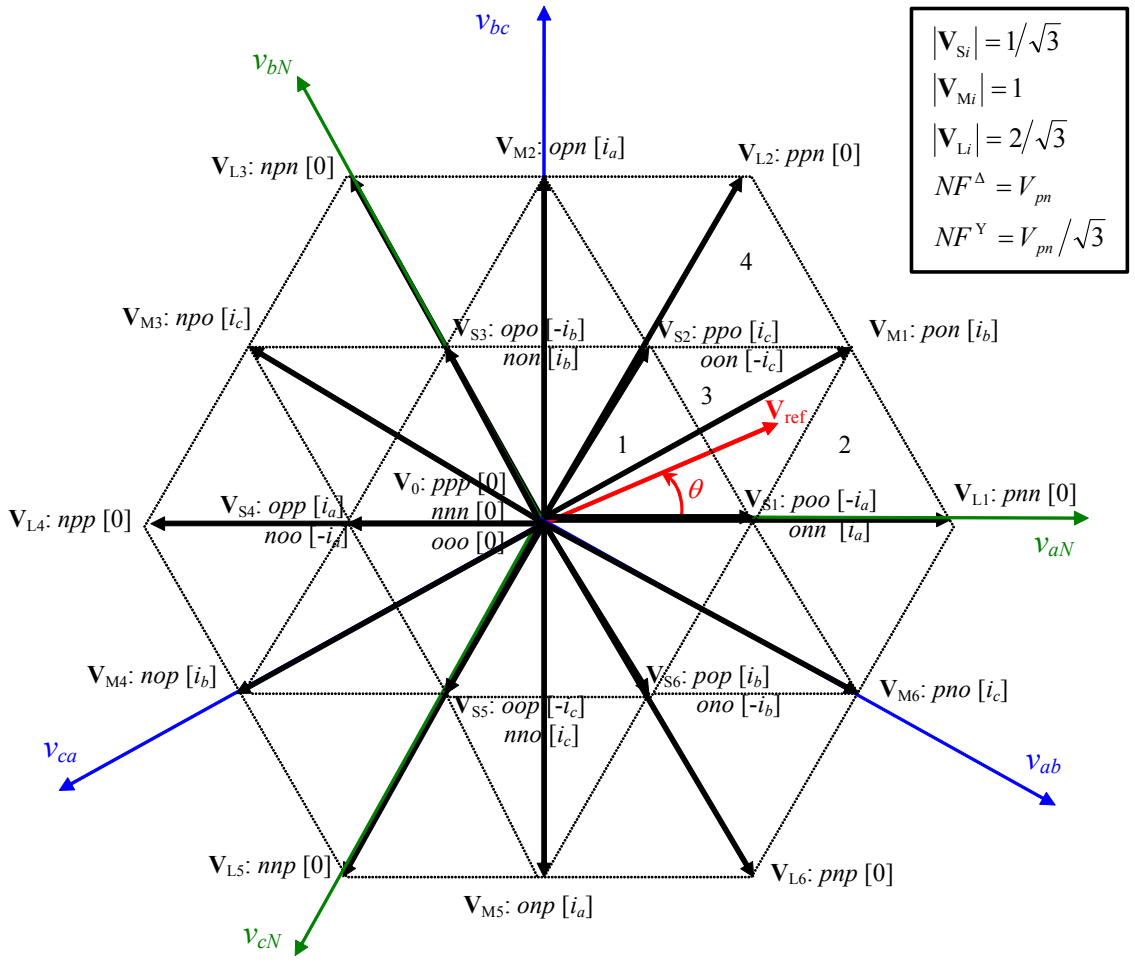


Fig. 1.3. Normalized SVD for the 3L-3P NPC dc-ac converter.

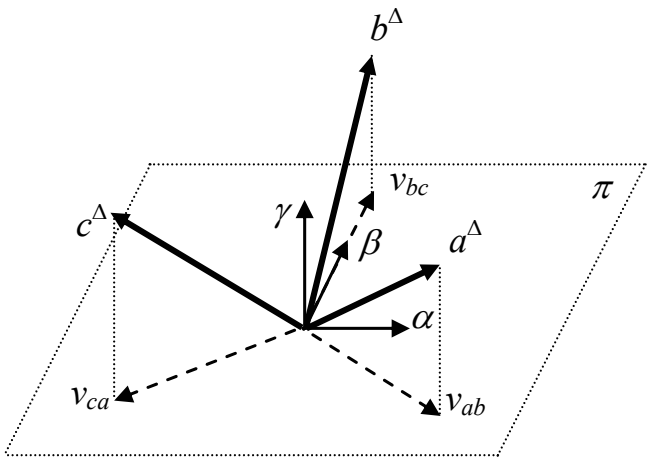


Fig. 1.4. Canonical a^{Δ}-b^{Δ}-c^{Δ} axis set and plane π.

The three-level NPC converter has 27 switching states corresponding to all the combinations of connections of each phase to the dc-link points *p*, *o*, and *n*; e.g., *pno*, corresponding to the connection of phase *a* to point *p*, phase *b* to *n*, and phase *c* to *o*. These switching states define 19 space vectors in the diagram of Fig. 1.3, classified as zero ($\mathbf{V}_0$), small ($\mathbf{V}_{Si}$), medium ($\mathbf{V}_{Mi}$), and large ($\mathbf{V}_{Li}$), where i = 1, 2…6. The orthogonal projection of these vectors onto any line-to-line or line-to-neutral voltage axis, times the normalizing factor (NF^{Δ} for line-to-line voltages; NF^{Y} for line-to-neutral voltages) gives the value of the corresponding voltage. The rotating reference vector ($\mathbf{V}_{ref}$) = $m \cdot e^{j\theta}$, $\theta = \omega_o \cdot t = 2\pi \cdot f_o \cdot t$) represents the desired three-phase output voltage. It is synthesized in each switching cycle (with switching period $T_s = 1 / f_s$) by a sequence of the converter voltage space vectors such that the flux of the reference vector equals the flux of the selected sequence. For instance, if the tip of $\mathbf{V}_{ref}$ is in triangle 2, vectors $\mathbf{V}_{S1}$, $\mathbf{V}_{M1}$ and $\mathbf{V}_{L1}$ could be chosen. Then,

$$\begin{aligned} &\mathbf{V}_{ref} = d_{\mathbf{V}S1} \cdot \mathbf{V}_{S1} + d_{\mathbf{V}M1} \cdot \mathbf{V}_{M1} + d_{\mathbf{V}L1} \cdot \mathbf{V}_{L1} \\ &0 \le d_{\mathbf{V}S1}, d_{\mathbf{V}M1}, d_{\mathbf{V}L1} \le 1 \\ &d_{\mathbf{V}S1} + d_{\mathbf{V}M1} + d_{\mathbf{V}L1} = 1 \end{aligned} \tag{1.1}$$

where $d_{\mathbf{V}S1}$, $d_{\mathbf{V}M1}$, and $d_{\mathbf{V}L1}$ correspond to the duty-ratio of vectors $\mathbf{V}_{S1}$, $\mathbf{V}_{M1}$, and $\mathbf{V}_{L1}$ in the particular switching cycle analyzed.

Whenever a vector can be generated by more than one switching state, an additional selection of one switching state or a combination of several has to be made. This is the case for the zero and small vectors. Finally, the sequence over time of the application of the selected converter switching states has to be decided for every switching cycle.

To define a modulation strategy, we need to select, for every possible modulation index *m* and for every switching cycle within one line-cycle of the reference vector, the voltage vectors we will use to synthesize $\mathbf{V}_{ref}$, the switching states we will use to produce those voltage vectors, and the sequence over time of the selected switching states. One can easily realize that there are a large number of possible modulation strategies.

Several modulation options have been explored. Most of them, both carrier-based and SVD-based, select the nearest-three space vectors (NTV) for every position of the reference vector. This typically guarantees a lower output-voltage harmonic distortion compared to other alternatives. Modulation solutions have been proposed in order to avoid narrow on and off pulses for the controlled devices [4], [7], [24], [39]; minimize the converter losses [8], [34], [39], [42]; minimize the output-voltage harmonic distortion [9], [11], [17]; and solve the neutral-point voltage balancing problem [19]-[45].

The narrow pulse problem is mainly relevant when gate turn-off thyristors (GTOs) are used. With the development of the isolated gate bipolar transistor (IGBT) technology in the past few years, providing devices with higher voltage ratings, this problem has become of a lesser importance.

The minimization of the converter losses is achieved through reducing the number of switching states applied per switching cycle and particularly avoiding those switching the phase carrying the highest current.

To characterize the output harmonic distortion and aid in the definition of modulation strategies, a novel figure, the harmonic distortion factor (*HDF*), based on a per switching-cycle evaluation of the harmonic flux, has been proposed [11]. However, while this figure provides a measure of the total harmonic distortion, it does not provide any insight into the distribution of harmonic levels within the output voltage spectra. There is also no explicit expression to compute the output voltage *THD* as a function of *HDF*.

Finally, a large number of contributions have concentrated on studying and solving an inherent problem in multilevel diode-clamped topologies: the neutral-point voltage balancing. Correct operation of the 3L NPC converter requires that the neutral-point voltage v_o be the average of the positive and negative voltages v_p and v_n. This is equivalent to say that the voltage across both dc-link capacitors (C_1 and C_2) must be the same. This ensures that the voltage stress that all semiconductors must withstand be the same, uniformly spreading the switching losses and improving the reliability. Let us define the dc-link capacitor voltage unbalance as the difference between the capacitor voltages and the corresponding balanced value:

$$v_{\text{unb}} = \frac{v_{C2} - v_{C1}}{2}. \tag{1.2}$$

On one hand, some authors study the response of the converter when having an unbalance in the line-cycle-average voltage across the dc-link capacitors [19], [20], [26], [27], [28], [32], [34], [37], [39], [40]. They investigate the inherent stability of the converter dc-link balance as a function of the modulation strategy and load, and propose a closed-loop control affecting the zero component of the output three-phase voltages [19], [20], [26] and other methods [27], [37] to eliminate those unbalances. As explained in [37] and [40], except for cases where the load introduces even and non-multiple of three current harmonics, the line-cycle-average unbalance is typically corrected naturally without the addition of any closed-loop control. The addition of such types of control, however, helps speed-up the process of recovering the line-cycle-average voltage balance of the dc-link capacitors.

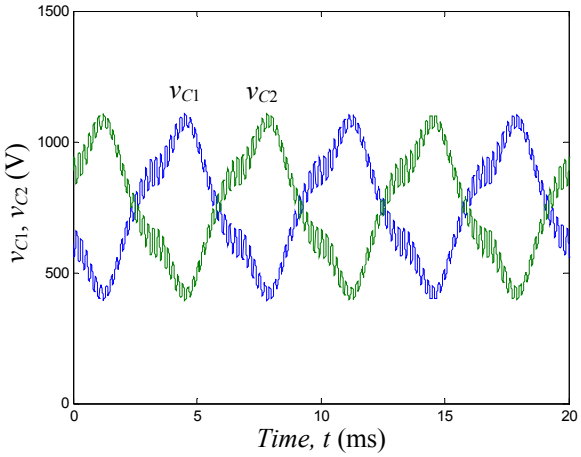
On the other hand, if conventional converter modulation strategies are applied to the three-level converter, a low-frequency (three times the fundamental frequency of the output voltage) oscillation of the capacitor voltages v_{C1} and v_{C2} occurs. For example, Fig. 1.5(a) depicts this oscillation for a NTV modulation used as a reference for comparison throughout the thesis (NTV50, see description in Chapter 2). The simulation has been performed with a small dc-link capacitance ($C_1 = C_2 = C_{dc} = 20$ μF) in order to highlight the dc-link unbalance and its effect on other variables. The neutral-point voltage oscillation increases the voltage stress on the devices. It also generates harmonics around the sixth-order harmonic in the output voltage (see Fig. 1.5(b)). The resulting load current also presents this low-frequency distortion (see Fig. 1.5(c)). Other load power factors may even increase the dc-link unbalance (see Fig. 1.6). A simple solution to this problem would be to increase the dc-link capacitors C_1 and C_2. But, in general, a significant increase in capacitance is required to satisfactorily suppress the low-frequency voltage oscillation, which not only means a significant increase in converter volume and cost but also a reduction in converter control bandwidth in applications where the system connected to the dc side behaves as a current source. For instance, and following with the previous example, Fig. 1.7 shows that for certain loading conditions a dc-link capacitance of 1 mF might be still causing a significant neutral-point voltage oscillation. Therefore, efforts have been directed towards solving this problem through defining an appropriate modulation pattern [22], [23], [24], [25], [28], [30], [31], [33], [38], [43], [45].

The neutral-point voltage balancing problem arises from the existence of a non-zero neutral-point-current i_o. If voltage V_{pn} is constant and $C_1 = C_2 = C_{dc}$, half of i_o flows through the upper capacitor and the remaining half through the lower capacitor, as shown in Fig. 1.8. This results in an unbalance of the dc-link capacitor voltages, since

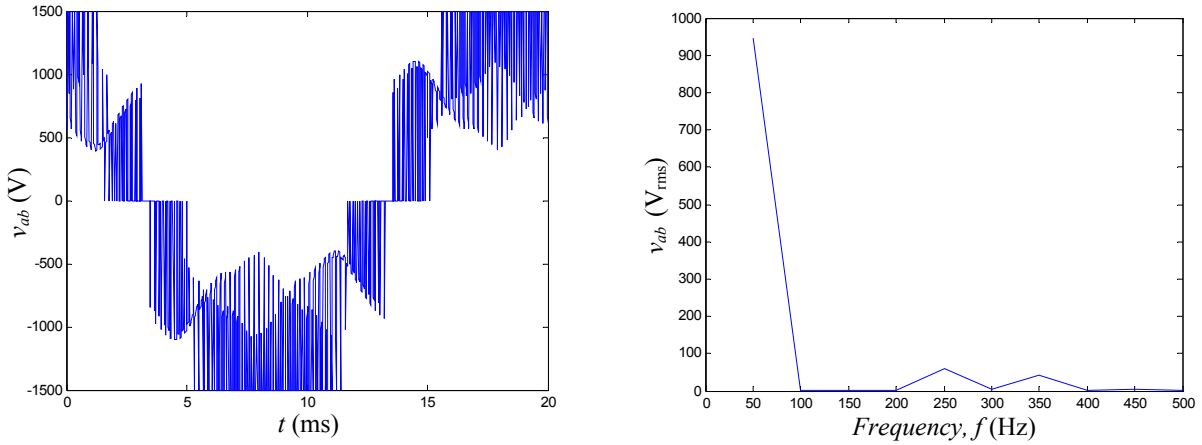
$$\frac{dv_{unb}}{dt} = \frac{\frac{dv_{C2}}{dt} - \frac{dv_{C1}}{dt}}{2} = \frac{-\frac{i_o}{2C_{dc}} - \frac{i_o}{2C_{dc}}}{2} = -\frac{i_o}{2C_{dc}}. \tag{1.3}$$

Each converter switching state in Fig. 1.3 causes a particular current i_o. These are specified in brackets in the diagram of Fig. 1.3. The switching states corresponding to the zero and large vectors introduce a current i_o equal to zero. The two switching states associated to a small vector introduce a current equal to a phase current but opposite in sign. Finally, the switching states producing middle vectors introduce an i_o equal to a phase current different from the phase currents introduced by neighboring small vectors.

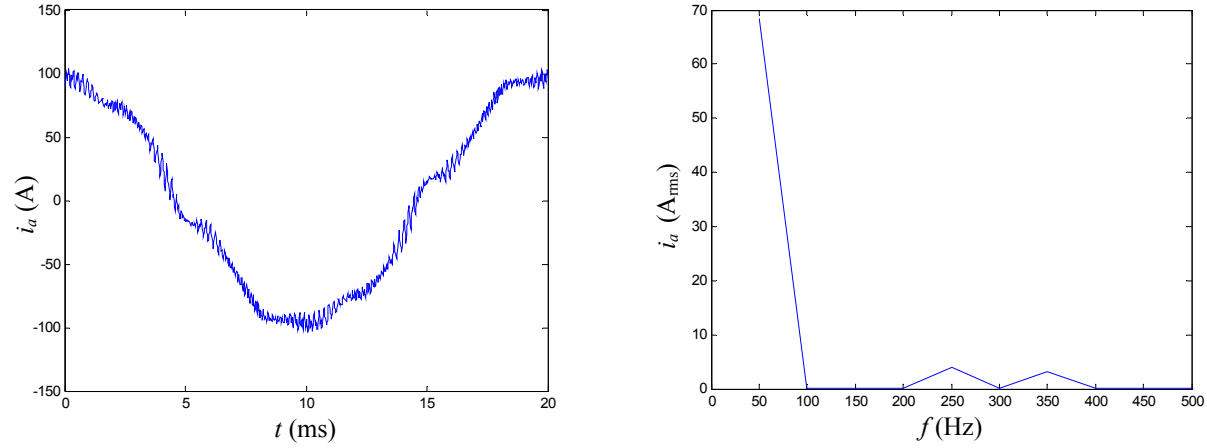
The objective is to define a modulation strategy such that the average i_o in every switching cycle equals zero. Most of the modulation solutions appearing in the literature select the NTV to



(a)



(b)



(c)

Fig. 1.5. Simulation results using a conventional NTV PWM, in the following conditions: V_{pn} *= 1500 V,* m *= 0.9,* f_o *= 50 Hz,* f_s *= 5 kHz,* C_{dc} *= 20 μF,* R_L *= 8 Ω,* C_L *= 0 F, and* L_L *= 1 mH. (a)* v_{C1} *and* v_{C2}*. (b)* v_{ab} *and* FFT(v_{ab})*. (c)* i_a *and* FFT(i_a)*.*

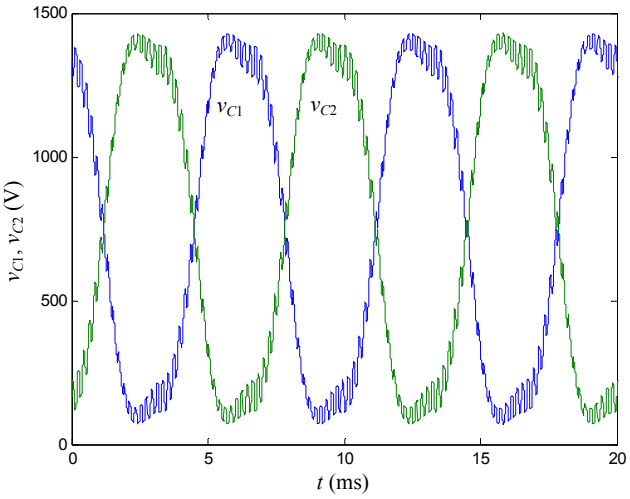


Fig. 1.6. Simulation results for v_{C1} and v_{C2}, using a conventional NTV PWM, in the following conditions: V_{pn} = 1500 V, m = 0.9, f_o = 50 Hz, f_s = 5 kHz, C_{dc}= 20 μF, R_L = 7.35 Ω, C_L = 0 F, and L_L = 10 mH.

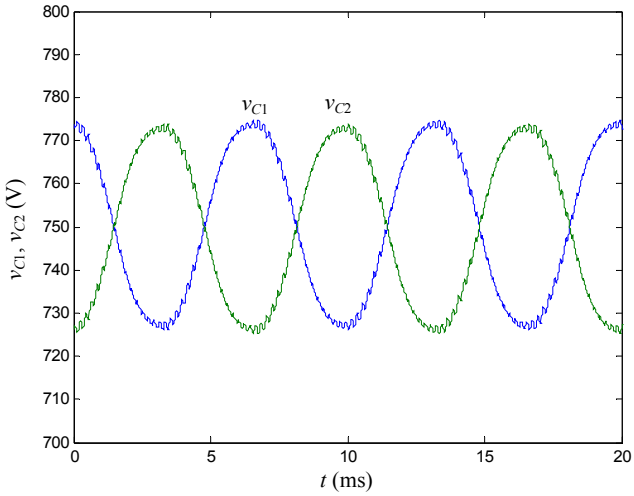


Fig. 1.7. Simulation results for v_{C1} and v_{C2}, using a conventional NTV PWM, in the following conditions: V_{pn} = 1500 V, m = 0.9, f_o = 50 Hz, f_s = 5 kHz, C_{dc}= 1 mF, R_L = 6 Ω, C_L = 0 F, and L_L = 15 mH.

synthesize the reference vector and then choose an appropriate combination of switching states for the small vectors in order to guarantee that the average i_o equals zero or to obtain a non-zero average i_o in order to correct any pre-existing unbalance. However, these solutions are unable to maintain the dc-link voltage balance for high modulation indexes and low power factors as demonstrated in [31]. The reason is that the neutral-point current introduced by middle vectors cannot be always fully compensated, in NTV modulations, by distributing the small vectors' duty-ratio into the two associated switching states. This problem has led some authors to introduce additional switching networks to guarantee the neutral-point voltage balancing [27], [36]. Other

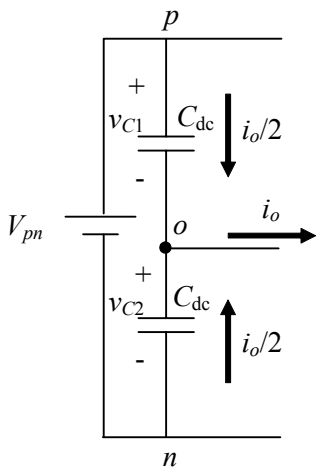


Fig. 1.8. Dc-link capacitor voltage unbalance due to a non-zero neutral-point current i_o.

authors [23], [25] propose modulation solutions eliminating the use of middle vectors. However, these modulations unnecessarily increase the output-voltage high-frequency distortion.

1.3. Objectives

The main objective of the proposed thesis is the definition and analysis of a new modulation strategy for the 3L-3P NPC converter. The desired performance characteristics of the modulation are:

- Comprehensive dc-link voltage balancing under any type of load: linear (balanced and unbalanced) and nonlinear, provided in all cases that the addition of the three phase currents equals zero.
- Minimum output three-phase voltage distortion at around the switching frequency.

A secondary objective of the proposed thesis is the definition of a new algebraic figure that allows incorporating the three-phase output-voltage distortion for any desired frequency band as a design parameter in the definition of PWM strategies for any multilevel inverter.

1.4. Thesis Outline

The thesis is organized as follows.

In Chapter 2, a new modulation, based on a virtual space vector concept, is proposed. This modulation achieves complete dc-link voltage balance for any load, provided that the addition of

the three phase currents equals zero. However, in the case of linear and balanced loads, the high-frequency output-voltage distortion generated by this modulation is not optimum.

Chapter 3 proposes then a new figure to characterize the output-voltage distortion of multilevel converters that can aid in the process of defining modulation strategies.

Chapter 4, starting from the modulation proposed in Chapter 2 and using the distortion figure derived in Chapter 3, presents an optimized modulation strategy, capable of controlling the neutral-point voltage with the minimum output-voltage distortion.

Chapter 5 discusses the issues involved in the closed-loop design of a 3L-3P NPC dc-ac converter using the proposed modulation. A specific loop is designed to control line-cycle average perturbations in the dc-link voltage balance and a complete control is designed for a particular application.

The thesis is concluded in Chapter 6, where possible future extensions of the work accomplished are also discussed.

Throughout the different chapters, experimental results are presented to validate the theoretical derivations and conclusions. Appendix A describes the experimental setup used for that purpose.

CHAPTER 2

NEAREST-THREE VIRTUAL-SPACE-VECTOR PULSEWIDTH MODULATION

Abstract — This chapter presents a new modulation approach for the complete control of the neutral-point voltage in the three-level three-phase neutral-point-clamped voltage source inverter. The new modulation approach, based on a virtual space vector concept, guarantees the balancing of the neutral-point voltage for any load (linear or nonlinear) over the full range of converter output voltage and for all load power factors, the only requirement being that the addition of the output three-phase currents equals zero. The implementation of the proposed modulation is simple according to the phase duty-ratio expressions presented. These expressions are only dependent on the modulation index and reference vector angle. The performance of this modulation approach and its benefits over other previously proposed solutions are verified through simulation and experiments.

2.1. Introduction

In this chapter, a novel PWM is defined. It is based on a virtual space vector (VV) concept and designated as the Nearest-Three Virtual-Space-Vector (NTV^2) PWM. The modulation is capable of controlling the neutral-point voltage over the full range of converter output voltage, for any load (linear or nonlinear), and for all load power factors. This solution was originally conceived in [47]. A similar concept of the VV has also been presented in [33], but the modulation presented there, applied to the direct torque control of an induction motor, differs from the one presented here in a few critical aspects; namely, in the definition of the VVs and in the selection of VVs in each switching cycle.

The chapter is organized as follows. In Section 2.2, the proposed modulation is defined. In Section 2.3, the corresponding phase duty-ratio expressions as a function of the modulation index and reference vector angle are presented in order to simplify the implementation of the proposed strategy. In Sections 2.4 and 2.5, the performance of the proposed modulation is analyzed and compared to a conventional modulation through simulation and experiments. Section 2.6 demonstrates the non-minimal high-frequency distortion of the proposed modulation under certain operating conditions and Section 2.7 outlines the conclusions.

2.2. Nearest-Three Virtual-Space-Vector Pulsewidth Modulation

2.2.1. Virtual Space Vector Definition

As seen in the previous chapter, in a conventional NTV PWM, the reference vector ($\mathbf{V}_{ref}$) is synthesized in each switching cycle by a sequence of the nearest three vectors. Whenever a vector can be generated by more than one switching state, an additional selection of one switching state or a combination of several has to be made. This is the case for the zero and small vectors.

In the diagram of Fig. 1.3, the neutral-point current corresponding to each switching state is specified in brackets. As stated earlier [31], the average i_o in a switching cycle must be zero to avoid a noticeable variation of the neutral-point voltage. The appropriate combination of switching states must be selected for the small vectors in order to achieve this goal, but as seen earlier [31], this is not possible when the modulation index m is high and for low load power factors. This is due to the fact that in these conditions, the current i_o introduced by medium vectors cannot be fully compensated by the current i_o introduced by small vectors.

To achieve full control of the neutral-point voltage, a set of new virtual vectors is defined as a linear combination of the vectors corresponding to certain switching states. The new virtual vectors ($\mathbf{V}_{Z0}$, $\mathbf{V}_{ZSi}$, $\mathbf{V}_{ZMi}$, and $\mathbf{V}_{ZLi}$), i = 1, 2…6, shown in Fig. 2.1 for the first sextant of the SVD, have an associated average i_o in each switching cycle equal to zero. This is true since:

1) $\mathbf{V}_{Z0}$ is obtained from switching state *ooo*, having an associated i_o equal to zero.

2) $\mathbf{V}_{ZSi}$ are obtained from an equitable combination of two switching states having the same associated i_o but opposite in sign. For example, if vector $\mathbf{V}_{ZS1}$ is selected for a period of time Δt, switching state *onn* will be active for $(1/2)\cdot\Delta t$, and *poo* will be active for the remaining $(1/2)\cdot\Delta t$. Therefore, the average i_o in Δt will be: $(1/\Delta t)\cdot[(1/2)\cdot\Delta t\cdot i_a+(1/2)\cdot\Delta t\cdot(-i_a)] = 0$.

3) $\mathbf{V}_{ZMi}$ are obtained from an equitable combination of three switching states having an associated i_o equal to i_a, i_b, and i_c, respectively, and $i_a + i_b + i_c = 0$. For instance, if vector $\mathbf{V}_{ZM1}$ is selected for a period of time Δt, switching state *onn* will be active for $(1/3)\cdot\Delta t$, *pon* will be active for $(1/3)\cdot\Delta t$, and *ppo* will be active for $(1/3)\cdot\Delta t$. Therefore, the average i_o in Δt will be: $(1/\Delta t)\cdot[(1/3)\cdot\Delta t\cdot i_a + (1/3)\cdot\Delta t\cdot i_b + (1/3)\cdot\Delta t\cdot i_c] = 0$.

4) $\mathbf{V}_{ZLi}$ are obtained from the switching states that define $\mathbf{V}_{Li}$, having all of them an associated i_o equal to zero.

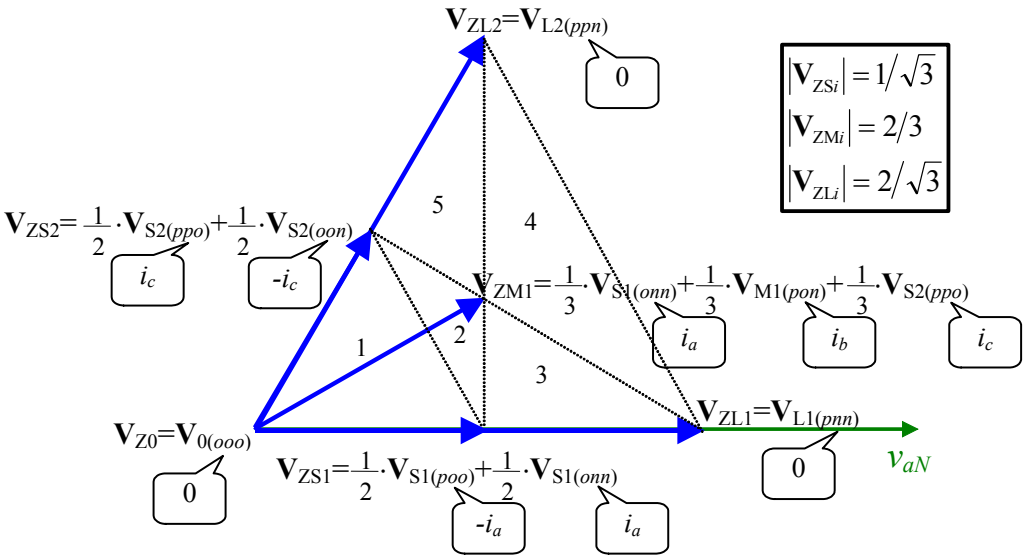


Fig. 2.1. VVs for the first sextant of the SVD.

2.2.2. Virtual Space Vectors Selection

The synthesis of the reference vector in each switching cycle is performed using the nearest three VVs. This defines five small triangular regions in the diagram of Fig. 2.1. Table 2.1 specifies the selected VVs in the cases where the tip of $\mathbf{V}_{ref}$ is in regions 1–5.

The duty ratio of each selected vector in each switching cycle is calculated as

$$\begin{aligned} &\mathbf{V}_{ref} = d_{\mathbf{VV}1}\cdot\mathbf{VV}_1 + d_{\mathbf{VV}2}\cdot\mathbf{VV}_2 + d_{\mathbf{VV}3}\cdot\mathbf{VV}_3 \\ &0 \le d_{\mathbf{VV}j} \le 1 \\ &d_{\mathbf{VV}1} + d_{\mathbf{VV}2} + d_{\mathbf{VV}3} = 1 \end{aligned} \tag{2.1}$$

where $\mathbf{VV}_j$ corresponds to the j^{th} selected VV (j = 1, 2, 3).

Region	Selected VVs
1	$\mathbf{V}_{Z0}$, $\mathbf{V}_{ZS1}$, $\mathbf{V}_{ZS2}$
2	$\mathbf{V}_{ZS1}$, $\mathbf{V}_{ZS2}$, $\mathbf{V}_{ZM1}$
3	$\mathbf{V}_{ZS1}$, $\mathbf{V}_{ZM1}$, $\mathbf{V}_{ZL1}$
4	$\mathbf{V}_{ZL1}$, $\mathbf{V}_{ZM1}$, $\mathbf{V}_{ZL2}$
5	$\mathbf{V}_{ZS2}$, $\mathbf{V}_{ZM1}$, $\mathbf{V}_{ZL2}$

Table 2.1. Selection of VVs for each triangular region.

The corresponding duty ratio of the different switching states can then be calculated. For the first sextant

$$\begin{aligned} d_{ooo} &= d_{\mathbf{V}Z0}, & d_{ppn} &= d_{\mathbf{V}ZL2} \\ d_{poo} &= (1/2)\cdot d_{\mathbf{V}ZS1}, & d_{pon} &= (1/3)\cdot d_{\mathbf{V}ZM1} \\ d_{oon} &= (1/2)\cdot d_{\mathbf{V}ZS2}, & d_{onn} &= (1/2)\cdot d_{\mathbf{V}ZS1} + (1/3)\cdot d_{\mathbf{V}ZM1} \\ d_{pnn} &= d_{\mathbf{V}ZL1}, & d_{ppo} &= (1/2)\cdot d_{\mathbf{V}ZS2} + (1/3)\cdot d_{\mathbf{V}ZM1}. \end{aligned} \tag{2.2}$$

2.2.3. Switching States Sequence

Finally, the sequence over time within a switching cycle of the application of the different switching states has to be decided. The chosen switching states' order is such that the sequence of connection of each phase to the dc-link points (*p*, *o*, and *n*) is the symmetrical *p-o-n-o-p*, as shown in Fig. 2.2.

Therefore, a practical implementation of the proposed modulation strategy only requires the computation of the independent duty ratios d_{ap}, d_{bp}, d_{cp}, d_{an}, d_{bn}, d_{cn} (where d_{xy} is the duty ratio of the phase *x* connection to the dc-link point *y*), as the addition of the appropriate switching state duty-ratios calculated in Section 2.2.2. For example, in the first sextant, to obtain d_{ap}

$$d_{ap} = d_{poo} + d_{pnn} + d_{ppn} + d_{pon} + d_{ppo}. \tag{2.3}$$

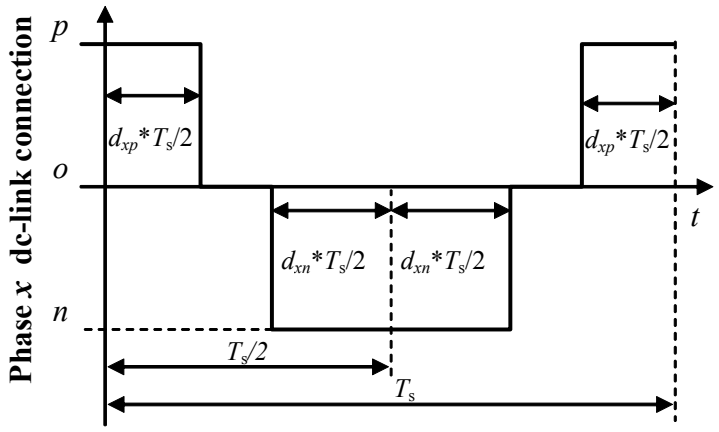


Fig. 2.2. Selected sequence of connection of phase x (a, b, or c) to each of the dc-link points (p, o, and n).

2.3. Phase Duty-Ratio Expressions

Fig. 2.3 shows the simulated duty ratios d_{ap} and d_{an}, for a line cycle and $m = 0.8$. The simple pattern observed for d_{ap} can be mathematically expressed as

$$\begin{aligned} &0 \le \theta < 2\pi/3: && d_{ap} = m \cdot \cos(\theta - \pi/6) \\ &2\pi/3 \le \theta < 4\pi/3: && d_{ap} = 0 \\ &4\pi/3 \le \theta < 2\pi: && d_{ap} = m \cdot \cos(\theta + \pi/6). \end{aligned} \tag{2.4}$$

The expression for duty ratio d_{an} is the same as (2.4) but phase-shifted 180°. The expressions for the duty-ratios of phases *b* and *c* are the same as for phase *a*, but phase shifted 120° and 240°, respectively. These expressions allow obtaining directly d_{ap}, d_{bp}, d_{cp}, d_{an}, d_{bn}, d_{cn} as a function of the modulation index *m* and reference vector angle θ, without the need of identifying the triangle in which the reference vector is located and then performing calculations (2.1)–(2.3). This significantly simplifies the computations.

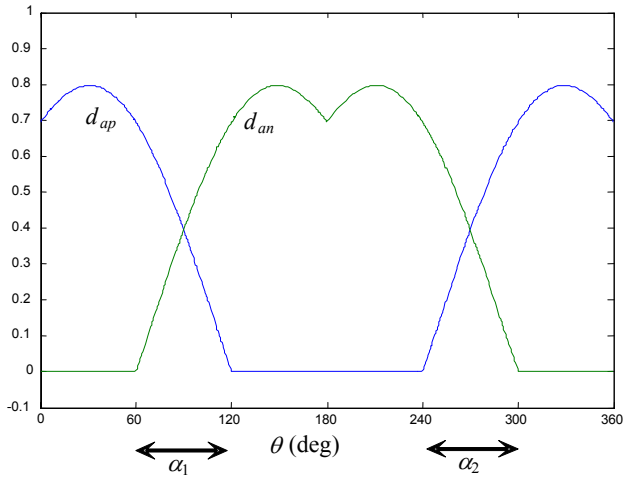


Fig. 2.3. d_{ap} and d_{an} as a function of θ ($m = 0.8$).

2.4. Simulation Results

2.4.1. Performance Evaluation at Nominal Operating Conditions

The performance of the proposed modulation has been verified through simulation in open loop using MATLAB/Simulink.

Fig. 2.4 shows the results obtained for the proposed NTV^2 PWM in what could be the nominal operating conditions of a 50 kW system. With a dc-link capacitance as small as 100 μF,

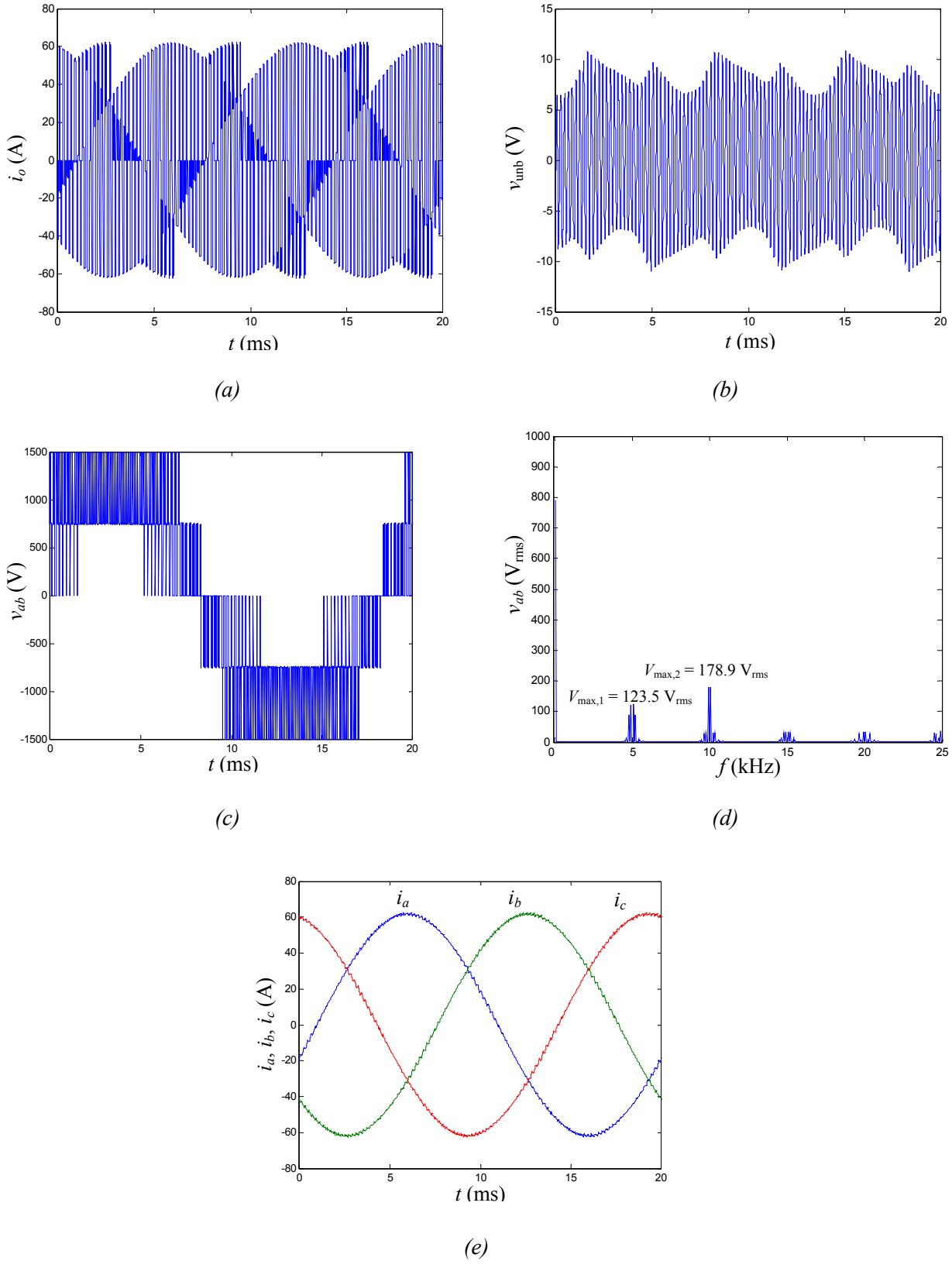


Fig. 2.4. Simulation results for the NTV² PWM in the following conditions: V_{pn} = 1500 V, m = 0.75, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 100 μF, R_L = 10 Ω, C_L = 0 F, and L_L = 10 mH (Load angle φ = 17.5°). (a) i_o. (b) v_{unb}. (c) Output voltage v_{ab}. (d) FFT(v_{ab}). (e) i_a, i_b, and i_c.

the neutral-point voltage oscillation is lower than 20 V, as seen in Fig. 2.4(b). Furthermore, the dc-link voltage unbalance does not present any low-frequency component. This leads to an output voltage free from any low-frequency components (see Fig. 2.4(d)).

2.4.2. NTV^2 vs. NTV

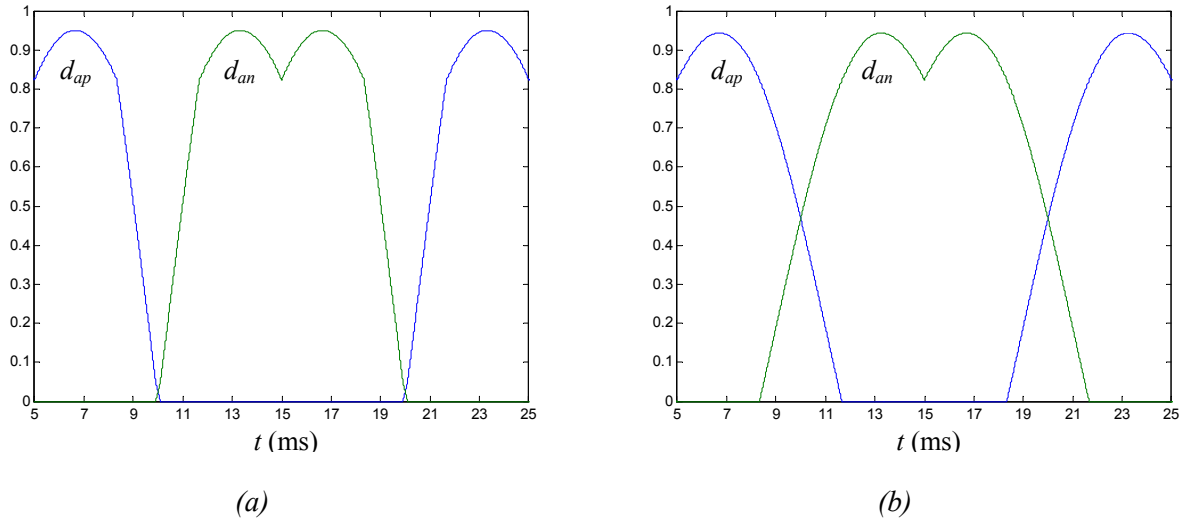
Figs. 2.5–2.7 compare the performance of a conventional NTV PWM and the proposed NTV^2 PWM. In the conventional NTV PWM considered for comparison, the duty ratio assigned to the small vectors is equally shared in every switching cycle by the corresponding two switching states, and $\mathbf{V}_0$ is implemented by switching state *ooo*. We designate this modulation as NTV50.

The comparison is performed at an operating point (m = 0.95, φ = 16º) where NTV strategies cannot control the neutral-point voltage. Fig. 2.5 presents the duty-ratio pattern for each modulation. The low-frequency neutral-point voltage oscillation incurred by the NTV50 PWM can be observed in Fig. 2.6(a). Instead, the proposed modulation completely controls the neutral-point voltage (Fig. 2.6 (b)). In fact, the NTV^2 PWM controls the neutral-point voltage for all modulation index m and load power factor. Note that since the average i_o in each switching cycle is zero, the switching-average i_o,

$$\langle i_o \rangle = \int_{t-T_s}^{t} i_o \cdot dt \tag{2.5}$$

presents a zero crossing every switching cycle.

However, this benefit in dc-link voltage balance is achieved at the expense of an increased output-voltage high-frequency distortion, as shown in Fig. 2.7.



(a) *(b)*

Fig. 2.5. Duty ratios d_{ap} and d_{an} (m = 0.95). (a) NTV50 PWM. (b) Proposed NTV^2 PWM.

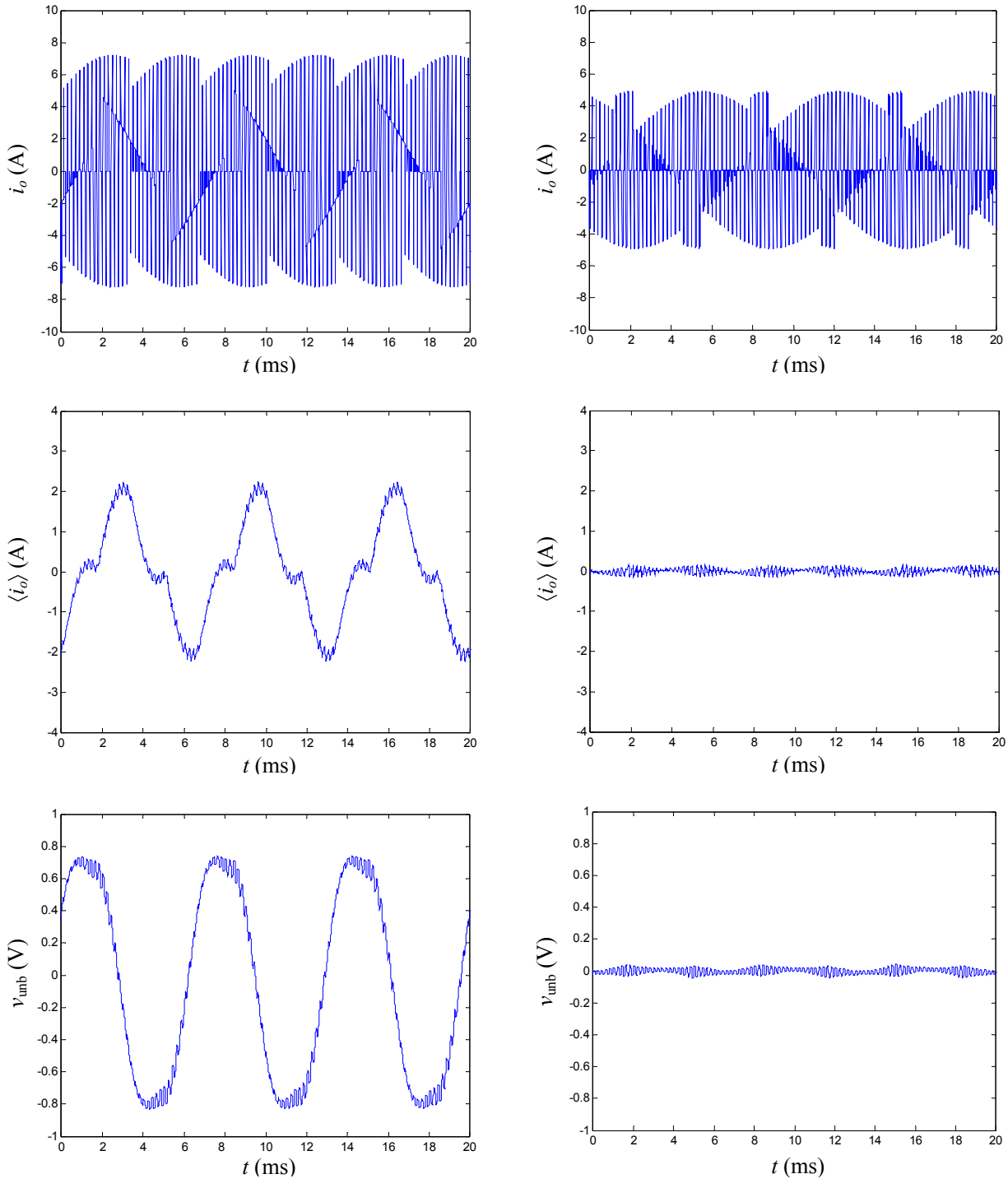


Fig. 2.6. Simulation results for i_o, switching-average i_o, and v_{unb} in the following conditions: V_{pn} = 150 V, m = 0.95, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 1.1 mF, R_L = 11 Ω, C_L = 0 F, and L_L = 10 mH (φ = 16°). (a) NTV50 PWM. (b) Proposed NTV² PWM.

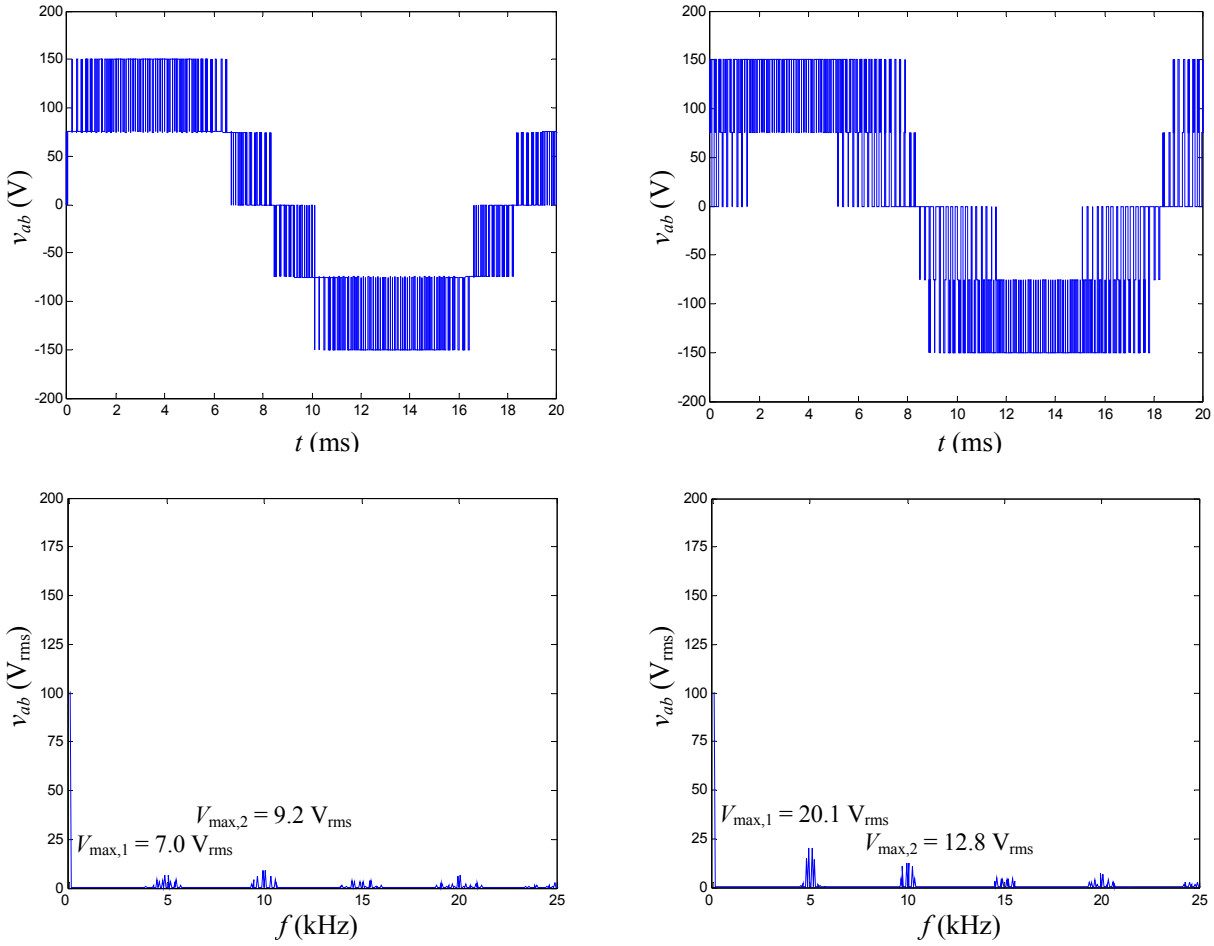


Fig. 2.7. Simulation results for output voltage v_{ab} and FFT(v_{ab}) *in the conditions of Fig. 2.6. (a) NTV50 PWM. (b) Proposed NTV² PWM.*

On the other hand, for the same switching frequency and high modulation indexes, the NTV² PWM requires 4/3 the number of commutations in the NTV50 PWM due to an additional commutation in regions α_1 and α_2 of Fig. 2.3. This increase in the number of commutations is due to the fact that the NTV² PWM always employs 5 different switching states per switching cycle, while the NTV50 PWM only uses 4 with high modulation indexes and for the majority of switching cycles. These additional commutations lead to an increase in switching losses. To evaluate the impact of this increase in losses, the thermal performance of both modulations has been analyzed through simulation.

First of all, we need to choose a converter implementation and thermal scenario for the comparison. Fig. 2.8 shows a converter leg implemented using IGBTs. Each outer switch (S_i, i = 1, 2…6) is packaged together with its corresponding antiparallel diode (D_i, i = 1, 2…6) and the nearest clamping diode (D_{ci}, i = 1, 2…6) in what we call an A-type module. The two inner switches

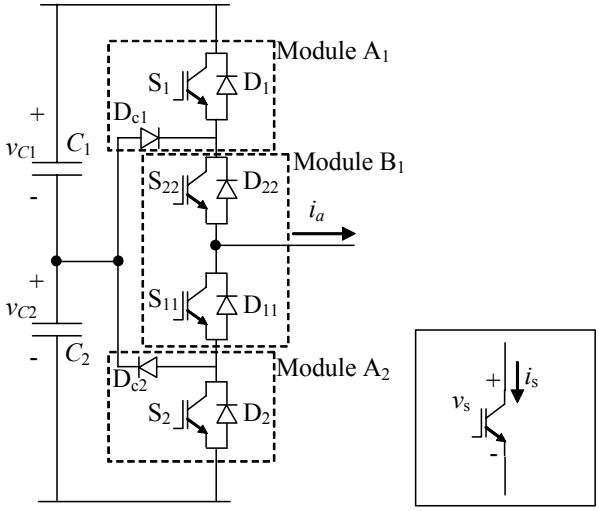


Fig. 2.8. Converter leg implemented using IGBTs.

of each leg (S_{ii}, i = 1, 2…6) together with their antiparallel diodes (D_{ii}, i = 1, 2…6) form a B-type module. Therefore, the whole converter can be built using six A-type modules (A_1 through A_6) and three B-type modules (B_1, B_2 and B_3). We will consider all nine modules attached to a common heat sink. Due to the symmetry in the converter configuration and mode of operation, all outer switches will have the same thermal performance. The same applies to all outer antiparallel diodes, to all inner switches, to all inner antiparallel diodes, and to all clamping diodes.

Fig. 2.9 presents the converter thermo-dynamical model. Only modules A_1 and B_1 are represented here. The model of the remaining modules is analogous. Each device has an associated power loss that flows through the corresponding thermal impedance to define the relevant device temperatures. The different model parameters and variables are:

p_{loss}: Switching-cycle averaged device power loss.

T_a: Ambient temperature.

T_h: Heat-sink temperature.

T_c: Case temperature.

T_i: Temperature at the point of common coupling of different devices integrated together.

T_j: Junction temperature.

R_{xy}: Thermal resistance between nodes x and y.

C_{xy}: Thermal capacitance between nodes x and y.

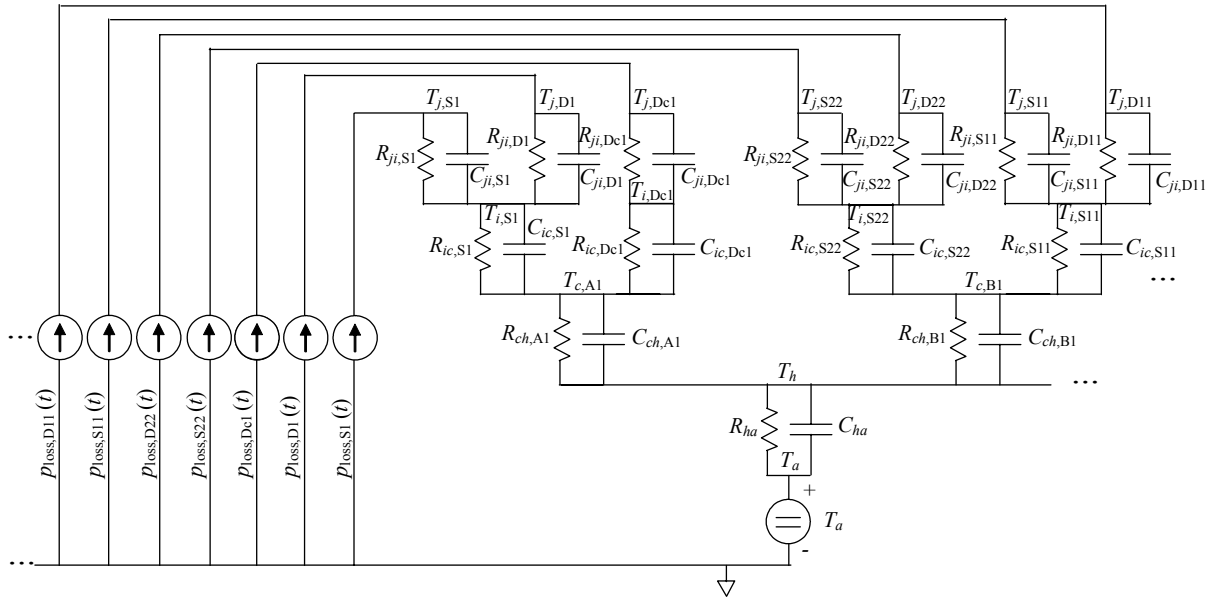


Fig. 2.9. Converter thermo-dynamical model.

The particular device or module to which these parameters and variables refer to is specified after the comma at the end of the variable subscript.

The IGBT power loss has been estimated considering both conduction (p_{cond}) and switching (p_{sw}) power loss. To compute the conduction losses, the switch is modeled as a constant voltage source with a series resistance. The estimation of the switching losses is performed assuming the simplified switch voltage-and-current waveforms of Fig. 2.10, corresponding to the turn-off and turn-on transitions in the case of an inductive load. For phase *a*, switch losses are calculated

$$p_{\text{loss}}(t) = p_{\text{cond}}(t) + p_{\text{sw}}(t)$$

$$\begin{aligned}
p_{\text{cond,S1}}(t) &= (i_a > 0)\cdot d_{ap}\cdot i_a.(V_{\text{s}} + R_{\text{s}}\cdot i_a)\\
p_{\text{sw,S1}}(t) &= (i_a > 0)\cdot (d_{ap} > 0)\cdot i_a \cdot v_{C1}\cdot t_{\text{sw}}\cdot f_{\text{s}}\\
p_{\text{cond,S22}}(t) &= (i_a > 0)\cdot (d_{ap} + d_{ao})\cdot i_a.(V_{\text{s}} + R_{\text{s}}\cdot i_a)\\
p_{\text{sw,S22}}(t) &= (i_a > 0)\cdot (d_{an} > 0)\cdot i_a \cdot v_{C2}\cdot t_{\text{sw}}\cdot f_{\text{s}}\\
p_{\text{cond,S11}}(t) &= (i_a < 0)\cdot (d_{an} + d_{ao})\cdot |i_a|.(V_{\text{s}} + R_{\text{s}}\cdot |i_a|)\\
p_{\text{sw,S11}}(t) &= (i_a < 0)\cdot (d_{ap} > 0)\cdot |i_a| \cdot v_{C1}\cdot t_{\text{sw}}\cdot f_{\text{s}}\\
p_{\text{cond,S2}}(t) &= (i_a < 0)\cdot d_{an}\cdot |i_a|.(V_{\text{s}} + R_{\text{s}}\cdot |i_a|)\\
p_{\text{sw,S2}}(t) &= (i_a < 0)\cdot (d_{an} > 0)\cdot |i_a| \cdot v_{C2}\cdot t_{\text{sw}}\cdot f_{\text{s}}.
\end{aligned} \tag{2.6}$$

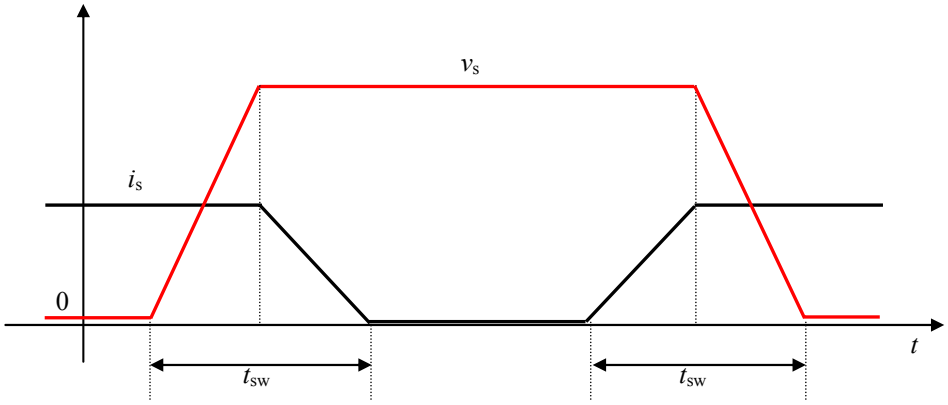


Fig. 2.10. Switch voltage-and-current simplified pattern to estimate switching losses.

The diode power loss has been estimated considering only conduction losses. In particular, no reverse recovery losses have been included. For phase *a*, diode losses are calculated

$$\begin{aligned} p_{\text{loss,D1}}(t) &= p_{\text{loss,D22}}(t) = (i_a < 0)\cdot d_{ap}\cdot |i_a|.(V_\text{d} + R_\text{d}\cdot |i_a|) \\ p_{\text{loss,D11}}(t) &= p_{\text{loss,D2}}(t) = (i_a > 0)\cdot d_{an}\cdot i_a\cdot (V_\text{d} + R_\text{d}\cdot i_a) \\ p_{\text{loss,Dc1}}(t) &= (i_a > 0)\cdot d_{ao}\cdot i_a.(V_\text{d} + R_\text{d}\cdot i_a) \\ p_{\text{loss,Dc2}}(t) &= (i_a < 0)\cdot d_{ao}\cdot |i_a|.(V_\text{d} + R_\text{d}\cdot |i_a|). \end{aligned} \tag{2.7}$$

The power loss in each device from phases *b* and *c* will be the same as in the corresponding device from phase *a*, but phase-shifted ±120º.

The value of the different parameters has been estimated for the prototype in Fig. 1.2(b), from the data-sheet of SEMIKRON modules SKM 100 GB/GAL/GAR 123D and from previous experience in power devices thermal modeling:

T_a = 40ºC

$V_\text{s} = V_\text{d}$ = 1 V

$R_\text{s} = R_\text{d}$ = 20 mΩ

t_{sw} = 300 ns

$R_{ha} = R_{ch}$ = 0.05 K/W

R_{ic} = 0.1 K/W

$R_{ji,(\text{S}k,\text{S}kk)}$ = 0.1 K/W (k = 1, 2...6)

$R_{ji,(\text{D}k,\text{D}kk)}$ = 0.4 K/W (k = 1, 2...6)

$R_{ji,\text{D}ck}$ = 0.3 K/W (k = 1, 2...6)

C_{ha} = 1000 J/K

C_{ch} = 10 J/K

C_{ic} = 20 J/K

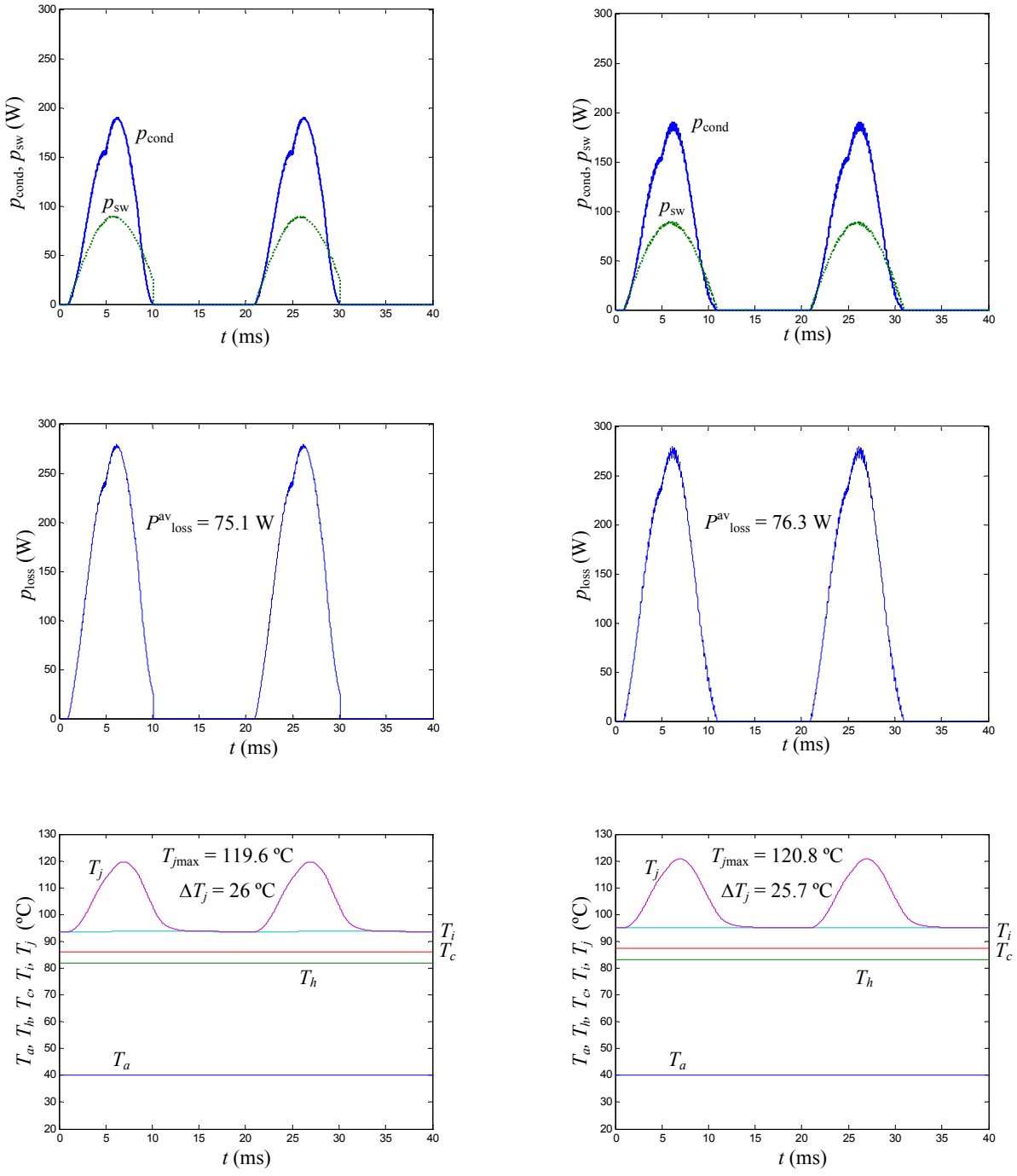
C_{ji} = 10 mJ/K. (2.8)

Figs. 2.11–2.15 show the simulation results for a particular inductive load and at a high modulation index (worst case) for the device's losses and converter temperatures with the NTV50 and NTV^2 PWM. Table 2.2 presents a summary of these results. Some observations can be made:

- At this operating point, the NTV^2 PWM has around 33 % more commutations than the NTV50 PWM, leading to a 13.4 % increase in switching losses. The percent increase in switching losses is lower than the percent increase in the number of commutations because the additional commutations occur at low current levels. The additional switching losses are concentrated on the least stressed switches.
- There is a transfer of conduction losses from the clamping diodes and inner switches to the outer switches, outer diodes, and inner diodes. This occurs due to a reduction of the connection to the neutral-point in favour of the connection to the *p* and *n* dc-link points: the conduction of a *clamping diode* + *inner switch* is replaced by the conduction of an *outer switch* + *inner switch* or an *outer diode* + *inner diode*. However, the overall conduction losses do not vary, since the same conduction model has been assumed for all devices. A big portion of these transferred conduction losses move to less stressed devices.
- As a result, there is only a 3 % increase in overall losses in the NTV^2 PWM compared to the NTV50 PWM.
- The heat-sink temperature suffers a slight increase due to this increase in overall losses.
- The switches maximum junction temperature ($T_{j\max}$) also slightly increases, but the thermal cycling stress (ΔT_j) is even lower due to the fact that the additional losses take place far away from the peak power lost and due to a general better switch utilization (losses better spread over the line cycle).
- The NTV^2 PWM presents a more uniform diode thermal stress.

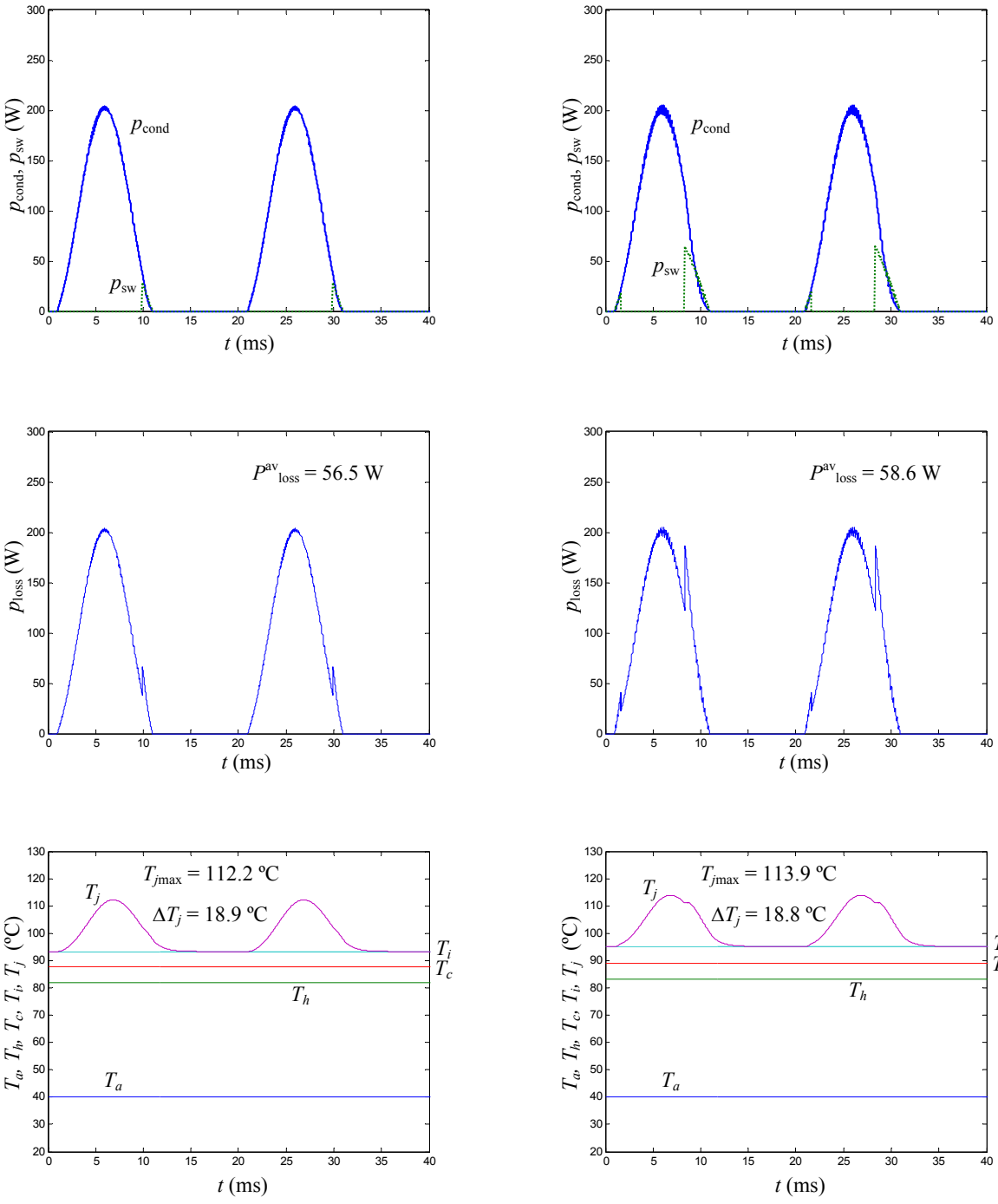
As a conclusion, under the operating conditions studied, the NTV^2 PWM does not present a significantly higher amount of losses and device junction temperature stress compared to the NTV50 PWM.

Fig. 2.16 presents the results obtained varying the inductive load angle. It can be seen that the losses and thermal stress with both modulations are similar for low load angles. This is less valid as the load angle increases because the additional switching transitions occur at higher current levels.



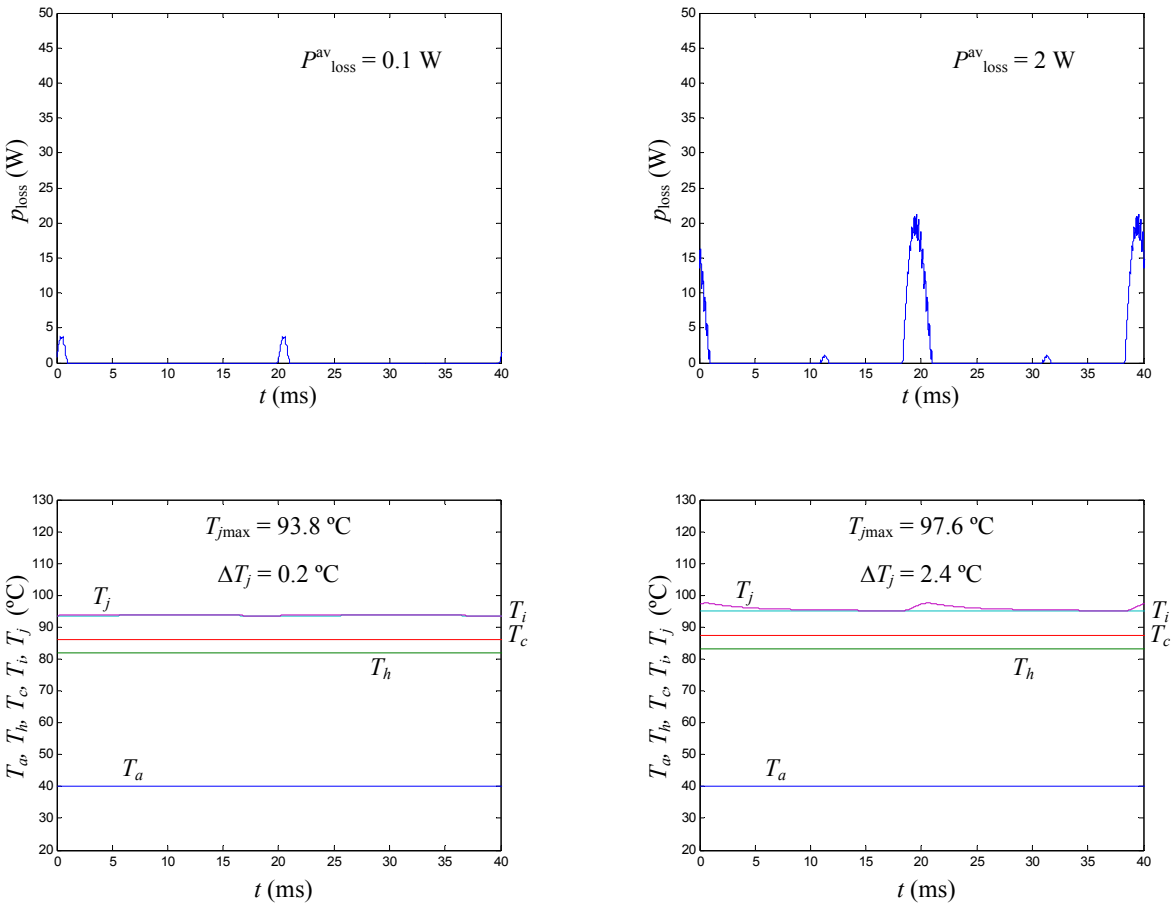
(a) *(b)*

Fig. 2.11. Outer switches (S_i, i = 1, 2…6). Conduction, switching, and total losses. Ambient, heat sink, and device temperatures. Conditions: T_a = 40 ºC, V_{pn} = 1500 V, m = 0.95, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 10 mF, R_L = 10 Ω, C_L = 0 F, and L_L = 10 mH (Load angle: φ = 17.5º, Output Power = 96 kW). (a) NTV50 PWM. (b) Proposed NTV² PWM.



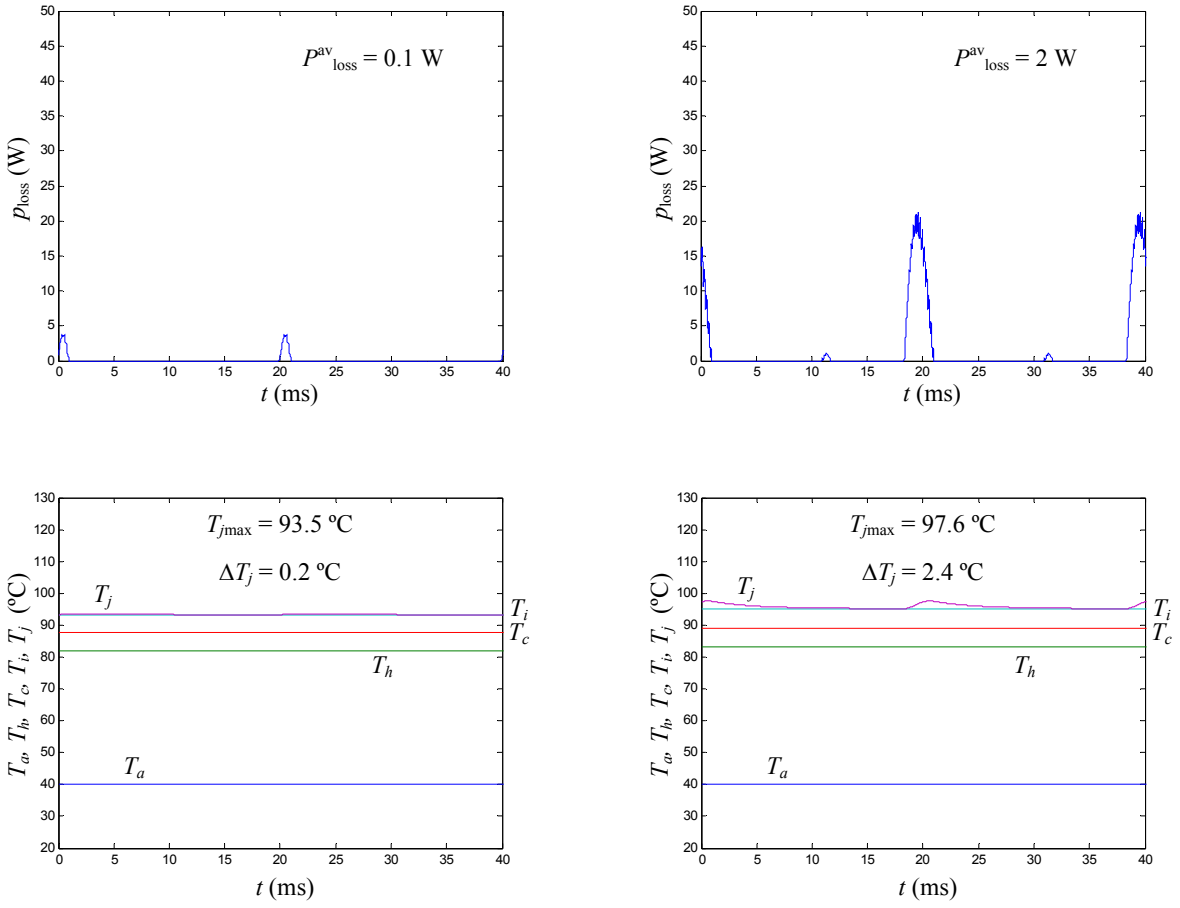
(a) *(b)*

Fig. 2.12. Inner switches (S_{ii}, i = 1,2…6). Conduction, switching, and total losses. Ambient, heat sink, and device temperatures. Same conditions as in Fig. 2.11. (a) NTV50 PWM. (b) Proposed NTV² PWM.



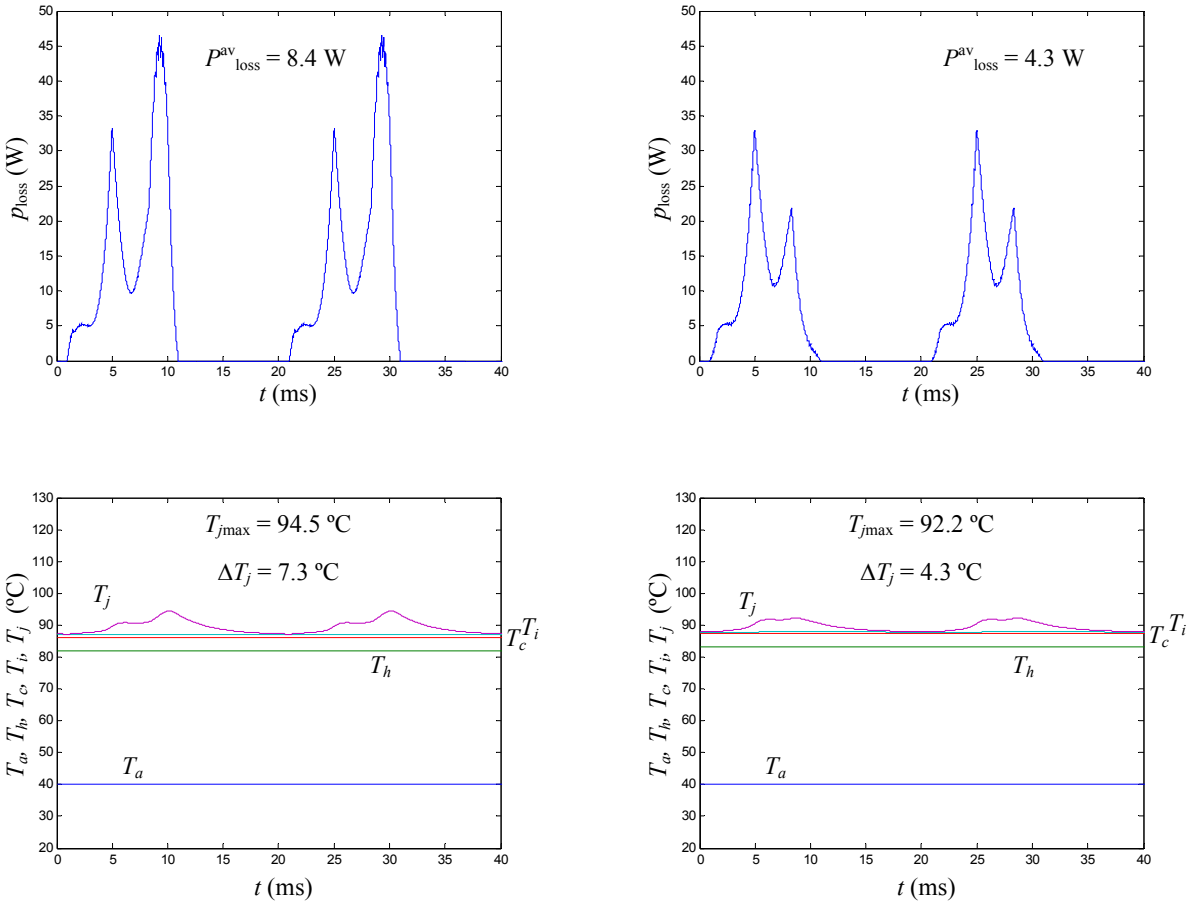
(a) *(b)*

Fig. 2.13. Outer diodes (D_i*, i = 1, 2…6). Total losses. Ambient, heat sink, and device temperatures. Same conditions as in Fig. 2.11. (a) NTV50 PWM. (b) Proposed NTV² PWM.*



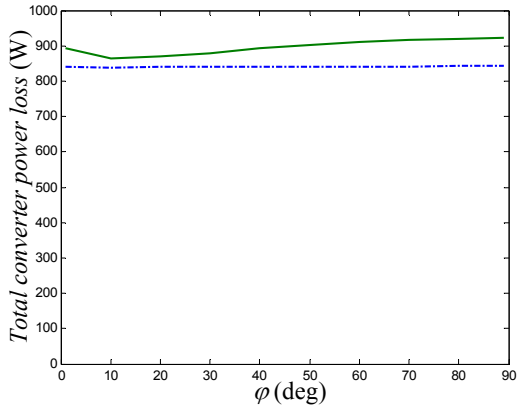
(a) *(b)*

Fig. 2.14. Inner diodes (D_{ii}, i = 1, 2…6). Total losses. Ambient, heat sink, and device temperatures. Same conditions as in Fig. 2.11. (a) NTV50 PWM. (b) Proposed NTV² PWM.

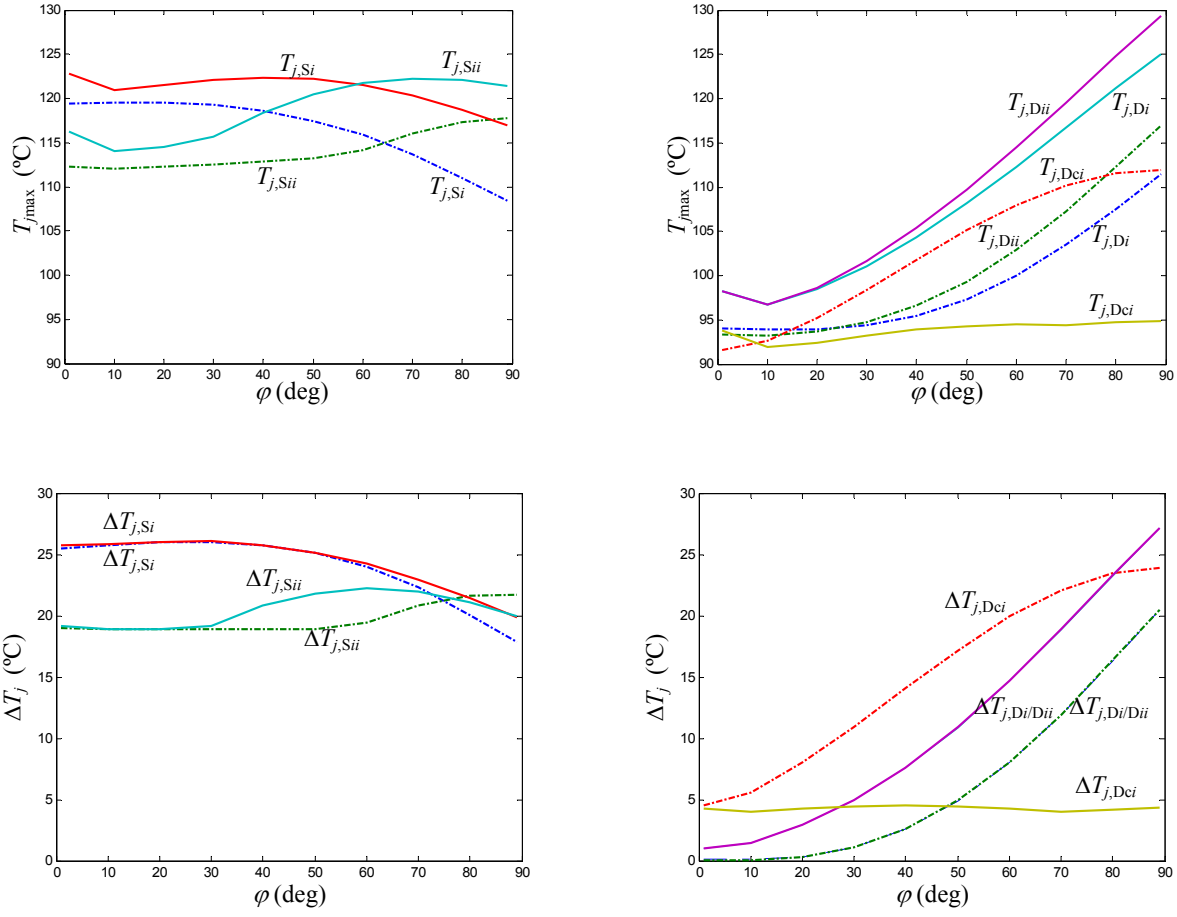


(a) *(b)*

Fig. 2.15. Clamping diodes (D_{ci}, i = 1, 2…6). Total losses. Ambient, heat sink, and device temperatures. Same conditions as in Fig. 2.11. (a) NTV50 PWM. (b) Proposed NTV² PWM.



(a)



(b) *(c)*

Fig. 2.16. Total converter power loss, maximum device junction temperature, and junction temperature variation as a function of the load angle. Conditions: Same conditions as in Fig. 2.11 and a fixed per-phase ac load impedance Z_L = 10.48 Ω. (a) Total converter power loss. (b) Outer and inner switches. (c) Outer, inner, and clamping diodes. (Dash-dot: NTV50 PWM. Solid: NTV² PWM)

NTV50 | NTV²	***Module A***			***Module B***		***Converter Total***
	Outer Switch	**Outer Diode**	**Clamping Diode**	**Inner Switch**	**Inner Diode**	
P^{av}_{cond} (W) *	47.4 | 48.3	0.1 | 2.0	8.4 | 5.5	55.8 | 53.8	0.1 | 2.0	670.8 | 669.6
P^{av}_{sw} (W)	27.7 | 28.0	----	----	0.7 | 4.8	----	170.4 | 196.8
P^{av}_{loss} (W)	75.1 | 76.3	0.1 | 2.0	8.4 | 5.5	56.5 | 58.6	0.1 | 2.0	841.2 | 866.4
T_h (ºC)	82.0 | 83.1					
T_c (ºC)	86.2 | 87.3			87.7 | 89.1		
T_{jmax} (ºC)	119.6 | 120.8	93.8 | 97.6	94.5 | 92.2	112.2 | 113.9	93.5 | 97.6	
ΔT_j (ºC)	26.0 | 25.7	0.2 | 2.4	7.3 | 4.3	18.9 | 18.8	0.2 | 2.4	

Table 2.2. Converter temp. and average losses for the NTV50 and NTV² PWM in the conditions of Fig. 2.11.

2.5. Experimental Results

The performance of the proposed modulation has been experimentally verified in open loop using the prototype shown in Fig. 1.2(b). Appendix A contains the details of the experimental setup. The modulator has been implemented using dSPACE 1103 and the EPF10K70 Altera FPGA (FLEX10K family). The PowerPC in the dSPACE 1103 board is in charge of computing d_{ap}, d_{bp}, d_{cp}, d_{an}, d_{bn}, d_{cn}, using (2.4) and the analogous equations for the remaining five duty ratios. This duty-ratio information is then sent to the FPGA, which is in charge of generating the control signals for the twelve inverter switches.

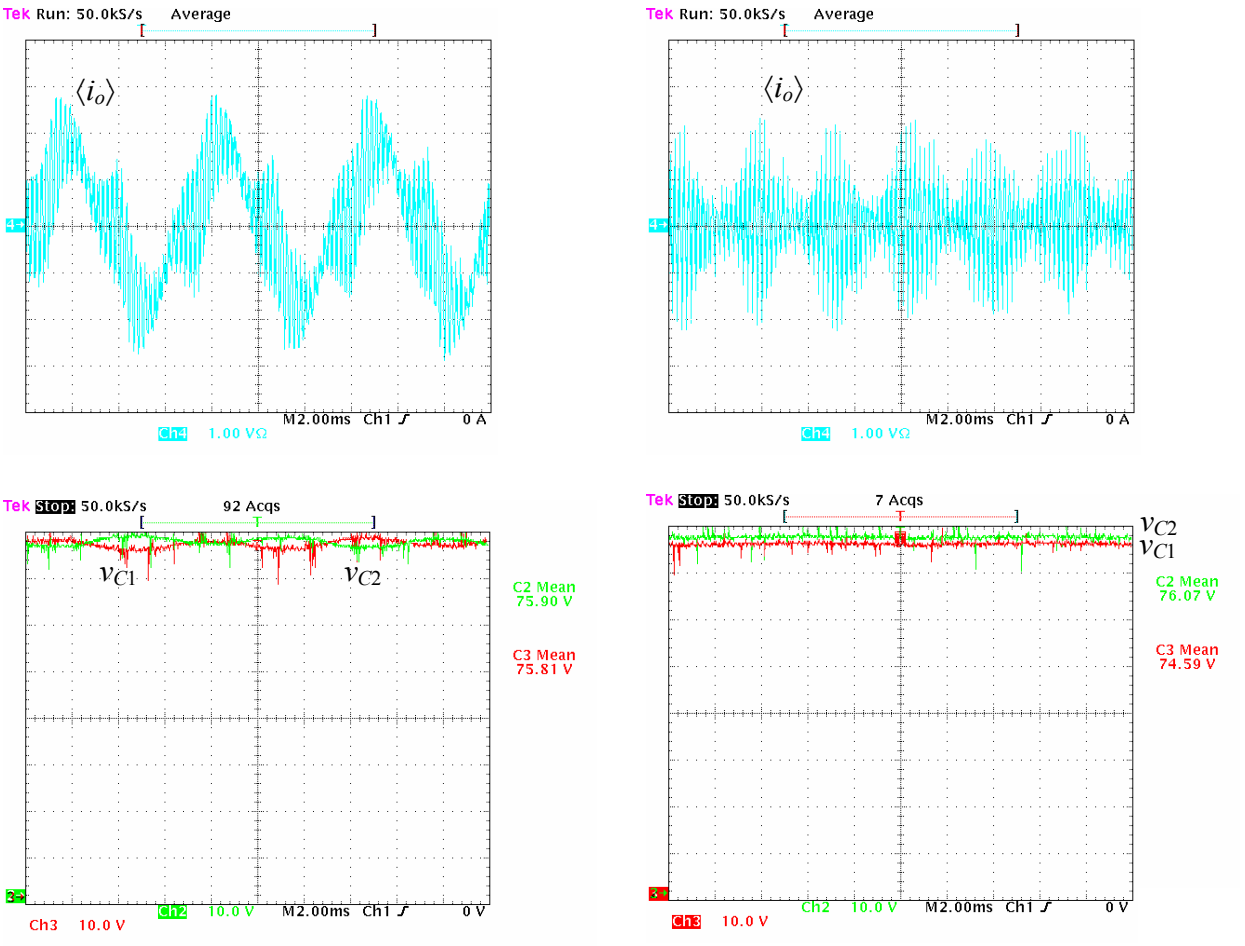
2.5.1. Ac-Side: Linear Load

2.5.1.1. Dc-Side: Dc-Voltage Power Supply

Figs. 2.17–2.18 show the experimental results obtained in the same conditions of the simulation results presented in Fig. 2.6. The first plot in Fig. 2.17 corresponds to the average capture, over 100 samples, of the neutral-point current i_o. The capture is triggered with the zero crossing of i_a. Since the triggering event occurs at different instants with reference to the line cycle, every point displayed corresponds to the average value of the samples captured over a time interval. This time interval happens to be in the order of the switching period. Hence, the waveform of the average capture of i_o is similar to $\langle i_o \rangle$. This plot shows that the average i_o in each switching

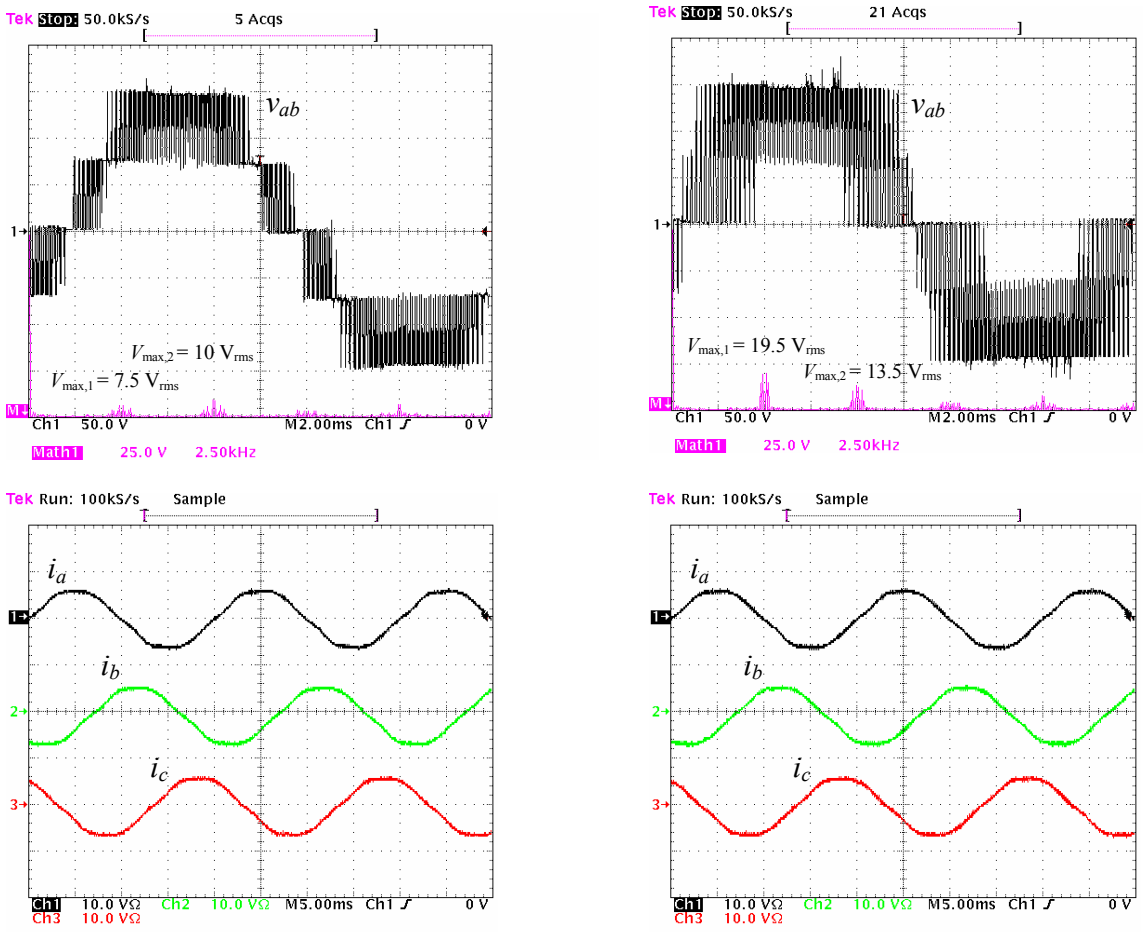
* Superscript 'av' indicates average value over a line cycle.

cycle is zero for the proposed modulation whereas it is not for the conventional solution. This is further verified from the fact that no low-frequency oscillations of the neutral-point voltage appear with the proposed modulation. Note that there is good agreement between the experimental and simulation results, reinforcing the conclusions derived before.



(a) *(b)*

Fig. 2.17. Experimental results for $\langle i_o \rangle$ [1 A/div], v_{C1}, and v_{C2} [10 V/div] in the following conditions: V_{pn} = 150 V, m = 0.95, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 1.1 mF, R_L = 11 Ω, C_L =0 F, and L_L = 10 mH (φ = 16°). (a) NTV50 PWM. (b) Proposed NTV² PWM.



(a) *(b)*

Fig. 2.18. Experimental results for output voltage v_{ab} [50 V/div], FFT(v_{ab}) *[25 V_{rms}/div], and output three-phase currents i_a, i_b, and i_c [10 A/div] in the same conditions of Fig. 2.17.*
(a) NTV50 PWM. (b) Proposed NTV² PWM.

2.5.1.2. *Dc-Side: Rectified Ac-Mains Voltage*

A rectified ac-mains voltage connected to the dc-link has also been tested (Fig. 2.19).

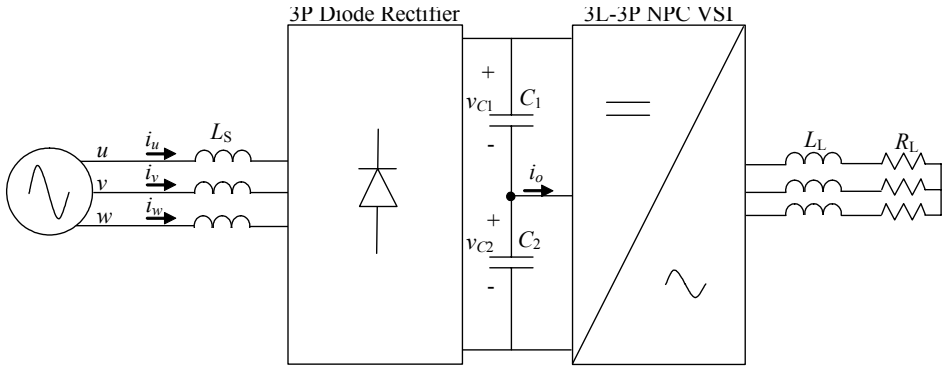


Fig. 2.19. Test configuration. Dc-side: rectified ac-mains voltage. Ac-side: linear load.

The results in Fig. 2.20 show that although there is an oscillation of the whole dc-link voltage $v_{C1} + v_{C2}$, there is no unbalance of the dc-link capacitor voltages. This is achieved thanks to the zero average i_o in each switching cycle, guaranteed by the modulation.

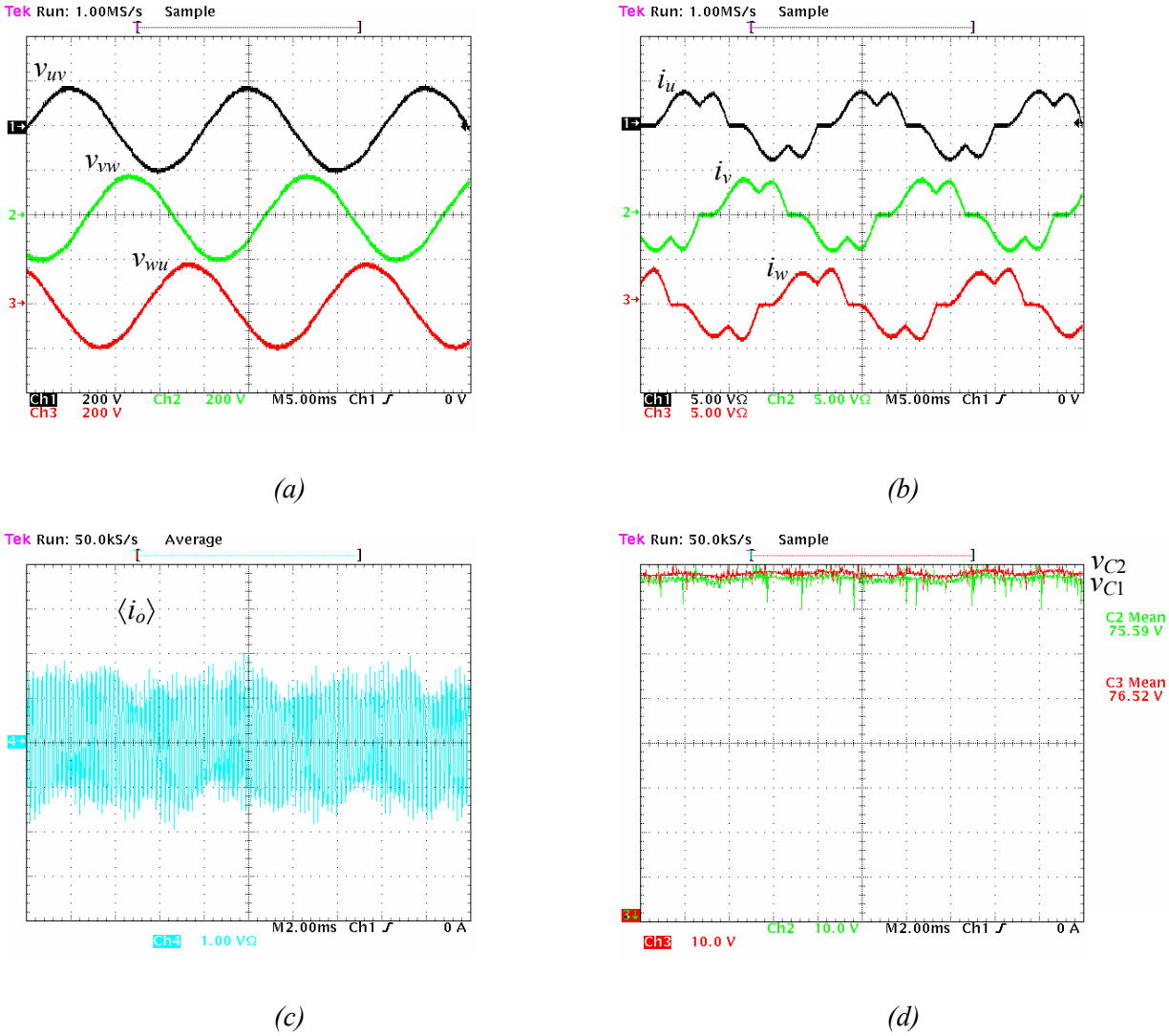


Fig. 2.20. Experimental results for the NTV² PWM in the following conditions:
L_S = 10 mH, m = 0.75, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 1.1 mF, L_L = 10 mH, and R_L = 11 Ω.
(a) v_{uv}, v_{vw}, v_{wu} [200 V/div]. (b) i_u, i_v, i_w [5 A/div]. (c) $\langle i_o \rangle$ [1 A/div]. (d) v_{C1} and v_{C2} [10 V/div].

2.5.1.3. Dc-Side: Rectified Generator Voltage

Under the test configuration in Fig. 2.21, where the rectified voltage of a generator is connected to the dc-link, the results (Fig. 2.22) are similar to those presented in the previous section. The dc-link is balanced despite of the dc-link capacitors low-frequency voltage ripple.

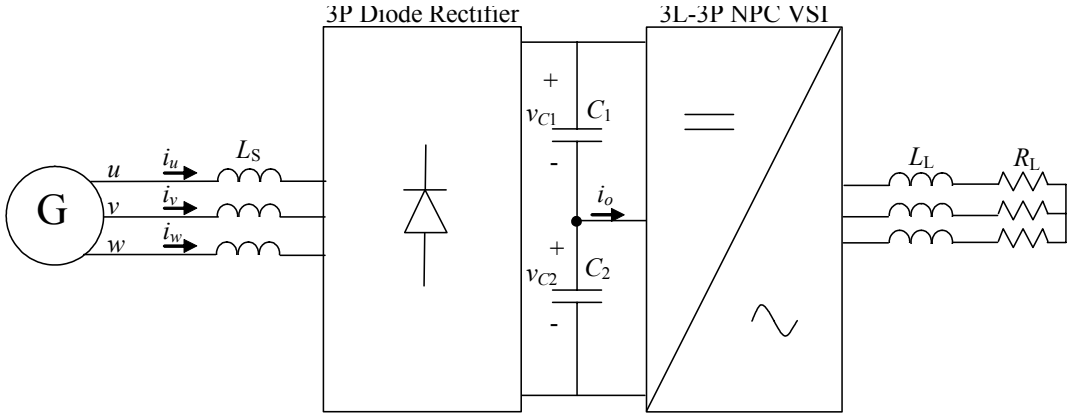
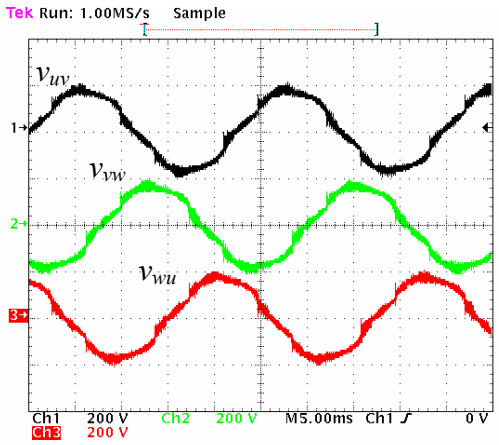
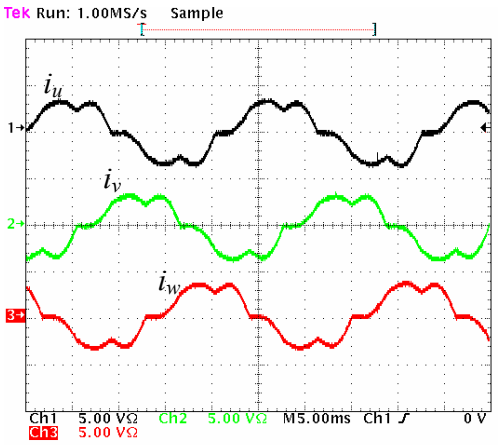


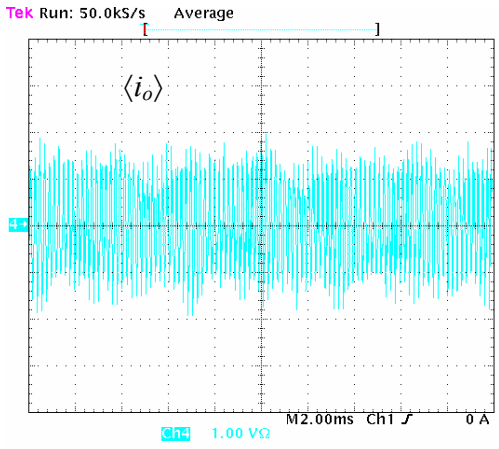
Fig. 2.21. Test configuration. Dc-side: rectified generator voltage. Ac-side: linear load.



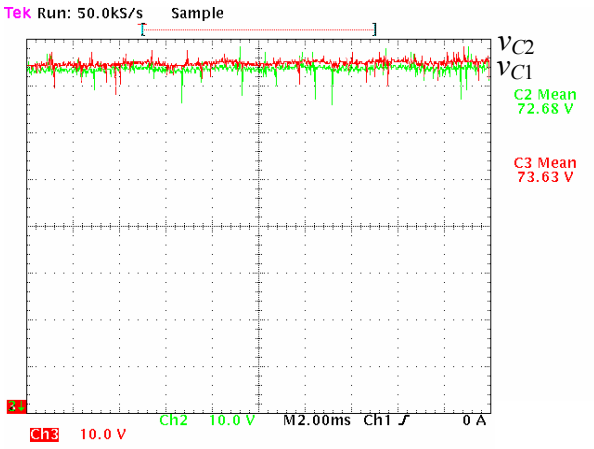
(a)



(b)



(c)



(d)

Fig. 2.22. Experimental results for the NTV² PWM in the following conditions:
L_S = 10 mH, m = 0.75, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 1.1 mF, L_L = 10 mH, and R_L = 16.5 Ω.
(a) v_{uv}, v_{vw}, v_{wu} [200 V/div]. (b) i_u, i_v, i_w [5 A/div]. (c) $\langle i_o \rangle$ [1 A/div]. (d) v_{C1} and v_{C2} [10 V/div].

2.5.2. Ac-Side: Non-Linear Load

The proposed modulation has also been tested with a non-linear load, consisting of an inductance, a three-phase diode rectifier, a capacitor and a resistor (Fig. 2.23). The results in Fig. 2.24 verify that the proposed modulation is capable of controlling the dc-link capacitor voltage balance, even under non-linear loading conditions.

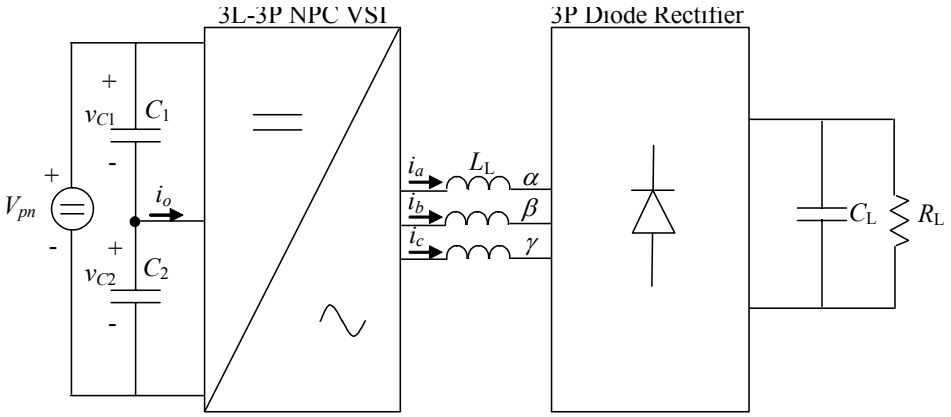


Fig. 2.23. Test configuration. Dc-side: dc-voltage power supply. Ac-side: non-linear load.

2.6. Non-Minimal High-Frequency Distortion

Fig. 2.25 presents the simulation results for the modulation strategy we designate as the Song PWM, proposed in [45]. The simulation has been performed in the same conditions we tested the NTV^2 PWM in Fig. 2.4 (m = 0.75; linear and balanced load with an angle φ = 17.5º). It can be clearly seen that the Song PWM is capable of controlling the neutral-point voltage with a lower high-frequency distortion of the output voltage, compared to the NTV^2 PWM.

The NTV^2 PWM is able to control the neutral-point voltage for any load (linear or non-linear) provided that $i_a + i_b + i_c = 0$. However, as seen in the previous comparison, under certain loading conditions (linear and balanced loads, low modulation indexes, and high load power factors), this control is achieved with a non-minimal output-voltage high-frequency distortion.

2.7. Conclusions

A new modulation approach for the comprehensive neutral-point voltage control in the 3L-3P NPC VSI has been presented. The dc-link capacitor voltage balancing is achieved for any load (linear or nonlinear) over the full range of converter output voltage and for all load power factors provided that $i_a + i_b + i_c = 0$. Thus, the proposed modulation allows reducing the size of the dc-link capacitors significantly.

The mathematical expressions of the phase duty-ratio have been derived, leading to a very compact computation implementation. These expressions are only dependent on the modulation index and reference vector angle. In particular, they do not depend on the load. Therefore, no knowledge of the load is required to implement the proposed modulation.

The benefits of the proposed solution over previous ones have been verified through simulation and experiments. These benefits are obtained at an expense of a higher output-voltage high-frequency distortion and higher number of switching transitions. The additional commutations do not lead to a significant increase in overall losses and thermal stress, especially at low $|\varphi|$.

Under certain operating conditions (linear-and-balanced loads, low modulation indexes and high load power factors), the proposed solution achieves complete control of the neutral-point voltage but with a non-minimal output-voltage high-frequency distortion.

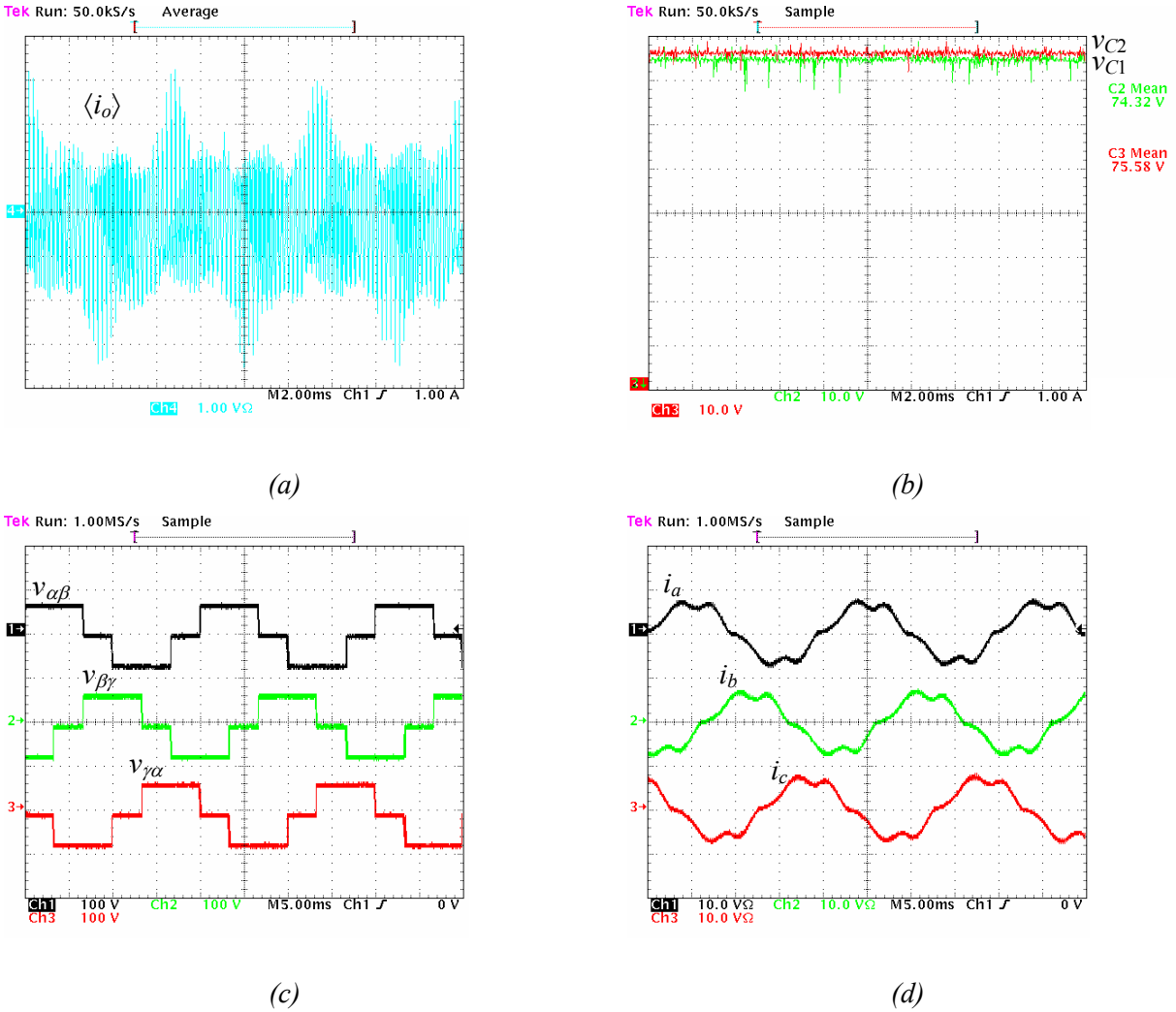


Fig. 2.24. Experimental results for the NTV² PWM in the following conditions:
V_{pn} = 150 V, m = 0.75, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 1.1 mF, L_L = 10 mH, C_L = 2 mF, and R_L = 11 Ω.
(a) ⟨i_o⟩ [1 A/div]. (b) v_{C1} and v_{C2} [10 V/div]. (c) $v_{\alpha\beta}$, $v_{\beta\gamma}$, $v_{\gamma\alpha}$ [100 V/div]. (d) i_a, i_b, i_c [10 A/div].

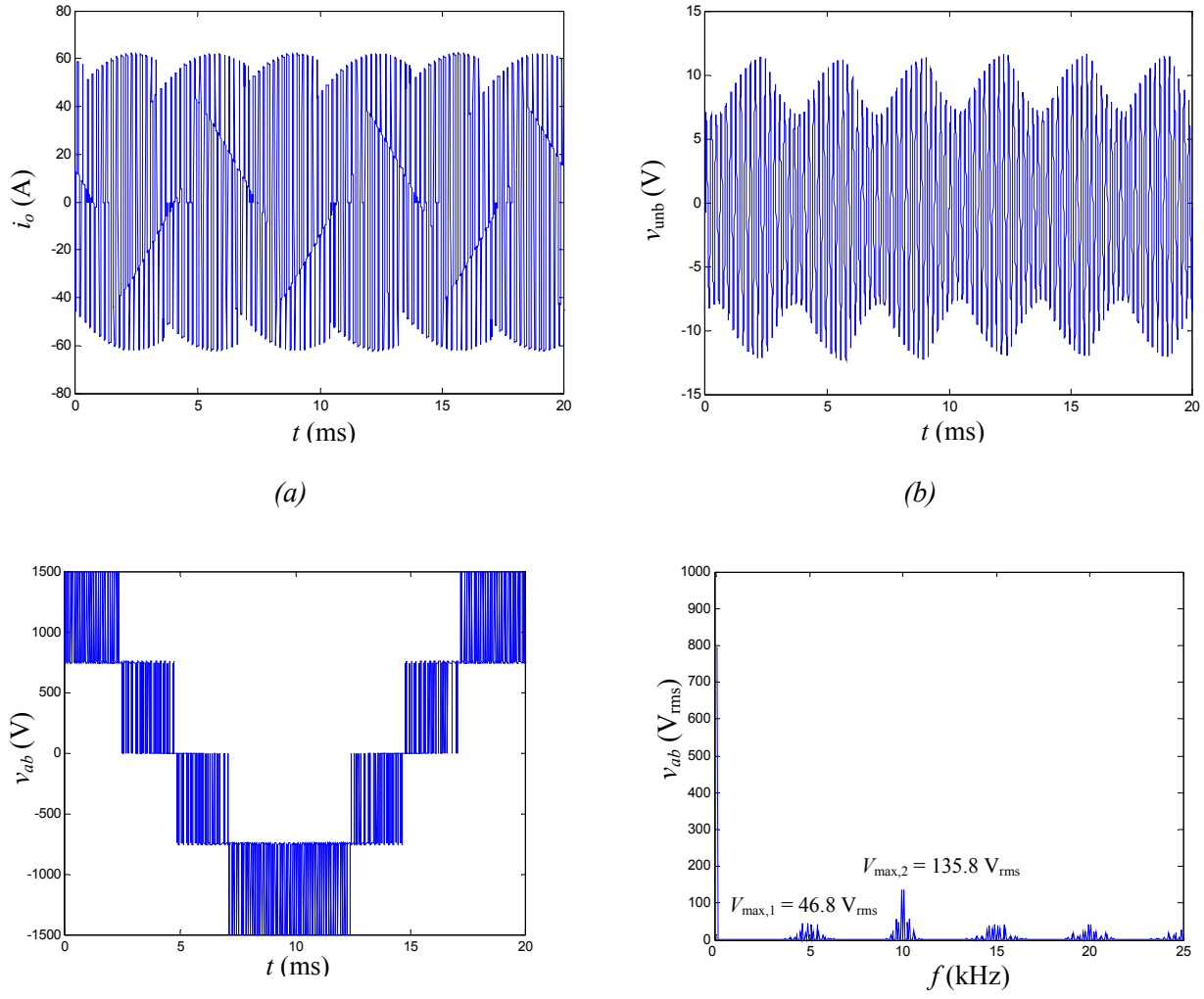


Fig. 2.25. Simulation results for the Song PWM in the conditions of Fig. 2.4: V_{pn} = 1500 V, m = 0.75, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 100 μF, R_L = 10 Ω, C_L = 0 F, and L_L = 10 mH (φ = 17.5°). (a) i_o. (b) v_{unb}. (c) Output voltage v_{ab}. (d) FFT(v_{ab}).

CHAPTER 3

OUTPUT-VOLTAGE DISTORTION CHARACTERIZATION IN MULTILEVEL PWM CONVERTERS

Abstract — One of the main features to consider in the development of new pulsewidth modulations for multilevel converters is the high-frequency output-voltage distortion. In this chapter, a novel per-switching-cycle figure, the harmonic distortion of order n for switching cycle k ($HD_{n,k}$), is introduced to quantitatively characterize the output three-phase voltage harmonic distortion of multilevel converters around all the integer multiples of the switching frequency. This figure allows decomposing the modulation design problem within an output voltage fundamental cycle into an independent set of smaller problems for every switching cycle. The expression of $HD_{n,k}$ as a function of the switching state duty-ratios is presented for the three-level three-phase neutral-point-clamped voltage source inverter and it can be easily obtained for any other multilevel converter.

From the evaluation of $HD_{n,k}$ over $1/6^{th}$ of the output-voltage fundamental-cycle the value of HD_n is obtained, providing a measure of the output-voltage distortion in a fundamental cycle. This information is obtained at a lower computational cost than conventional fast Fourier transform (FFT) analysis. The accuracy of the HD_n distortion predictions is verified through a comparison to FFT-based results obtained from simulation and experiments. The expression to compute the total harmonic distortion as a function of HD_n is also derived.

3.1. Introduction

One of the main features to consider in the evaluation of a given PWM strategy is the output-voltage harmonic distortion generated. This can be assessed by performing the fast Fourier transform (FFT) of the output line-to-line voltages, analyzing their spectra and, additionally, computing any desired distortion figure such as the total harmonic distortion (*THD*). However, there are computationally simpler methods of evaluating this distortion. For instance, [11] defines a harmonic distortion factor (*HDF*) which represents a quantitative measure of such distortion. It is based on the evaluation of the rms harmonic flux error in every switching cycle over $1/6^{th}$ of the output voltage fundamental cycle. Besides the lower number of computations required to evaluate the output voltage distortion, this approach has a more relevant benefit. The definition of a distortion figure in every switching cycle (the rms harmonic flux error) allows taking into account the output voltage distortion in the process of defining a modulation strategy, since this process is

usually, and for simplicity, performed step-by-step, starting with the first switching cycle, then following with the next, etc.

In this chapter, a new figure is proposed, the harmonic distortion of order n (HD_n), to quantitatively characterize the output voltage distortion in an output-voltage fundamental cycle. It is based on the evaluation of the distortion per switching-cycle k ($HD_{n,k}$) within $1/6^{th}$ of the output voltage fundamental cycle and provides a quantitative measure of the voltage harmonic distortion around all integer multiples of the switching frequency. Therefore, and compared to the *HDF*, it adds insight into the distribution of harmonic levels within the output voltage spectra. This is useful, for example, when searching for modulation strategies with a lower content of low-order harmonics which are more difficult to filter. An additional merit of the presented approach is that a simple expression allows computing the *THD* from the values of HD_n.

The chapter is organized as follows. In Section 3.2, the proposed figure, HD_n, applicable to any multilevel converter configuration, is defined. In Section 3.3, the simple algebraic expression defining HD_n as a function of the switching-state duty-ratios is derived for the case of the 3L-3P NPC VSI. In Section 3.4, the correspondence of the proposed figure value with the real distortion levels is verified through analysis of simulation and experimental results, and Section 3.5 outlines the conclusions.

3.2. HD_n: A New Approach to Voltage Harmonic Distortion Characterization

3.2.1. Error Vector Definition

Although the following concepts apply to any multilevel converter topology, for the sake of clarity and simplicity the explanation is based on the case of the 3L-3P NPC VSI (Fig. 1.2(a)). It is assumed that the dc-link voltages remain balanced: $v_{C1} = v_{C2} = V_{pn}/2$, either because the modulation strategy guarantees the balancing or because the dc-link capacitance $C_1 = C_2 = C_{dc}$ is large enough.

Fig. 3.1 presents the first sextant of the normalized SVD of the 3L-3P NPC VSI. The rotating reference vector $\mathbf{V}_{ref}$ (representing the desired three-phase output voltage) is synthesized with a PWM method, using a particular sequence of switching states *xyz* (where *x, y*, and *z* correspond to the dc-link points – *p*, *o* or *n* – to which phases *a*, *b*, and *c* are connected, respectively) within every switching cycle. That is, $\mathbf{V}_{ref}$ is approximated by a sequence of the available converter voltage space vectors. At any point in time *t*, we can define an error vector $\mathbf{V}_e$ as:

$$\mathbf{V}_e = \mathbf{V}_{app} - \mathbf{V}_{ref} \tag{3.1}$$

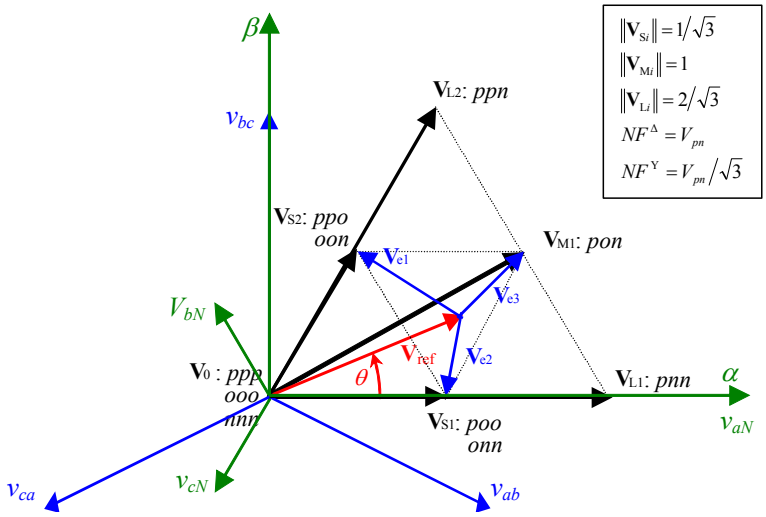


Fig. 3.1. First sextant of the normalized SVD of the 3L-3P NPC VSI.

where $\mathbf{V}_{app}$ corresponds to the applied voltage space vector at time *t*. For instance, $\mathbf{V}_{e3}$ in Fig. 3.1 corresponds to the error vector when the applied voltage space vector is $\mathbf{V}_{M1}$, corresponding to switching state *pon*.

3.2.2. Transformation of the Sequence of Error Vectors into a Series of Pulsating Vectors

In every switching cycle, $\mathbf{V}_{ref}$ is approximated using a particular sequence of switching states. Let us assume that in the particular position of $\mathbf{V}_{ref}$ in Fig. 3.1, switching states *ppo*, *poo* and *pon* are chosen. It is generally accepted that a symmetric sequence of switching states reduces the voltage distortion compared to any other sequence with the same number of commutations. Hence, the sequence of switching states within a switching cycle would be: *ppo*, *poo*, *pon, pon, poo, ppo.* The corresponding sequence of error vectors would be: $\mathbf{V}_{e1}$, $\mathbf{V}_{e2}$, $\mathbf{V}_{e3}$, $\mathbf{V}_{e3}$, $\mathbf{V}_{e2}$, $\mathbf{V}_{e1}$. This sequence of error vectors contains the information of the ripple in the output voltage for a given switching cycle. To obtain this ripple for any line-to-line voltage (or any line-to-neutral voltage), we project the sequence of error vectors into the corresponding axis and multiply by the corresponding normalizing factor (NF^{Δ} for line-to-line voltages; NF^{Y} for line-to-neutral voltages). For instance, Fig. 3.2 shows the ripple in v_{ab} (v^{r}_{ab}) corresponding to the particular switching cycle represented in Fig. 3.1.

The information contained in the sequence of error vectors can be translated to the frequency domain by the following transformation process:

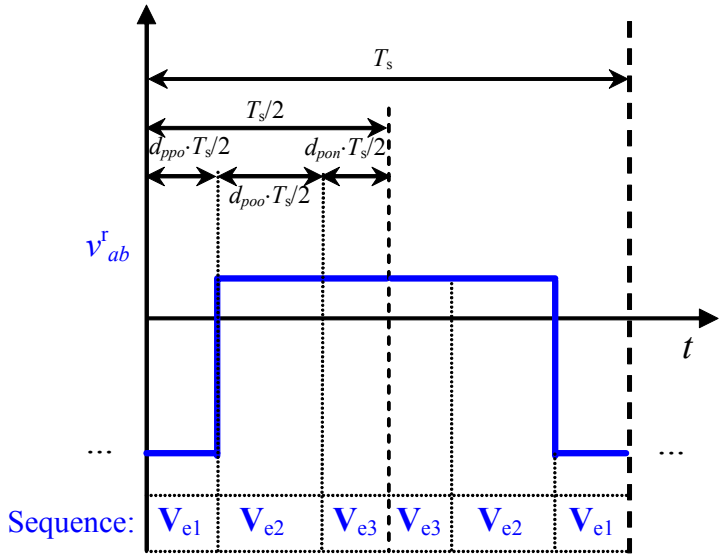


Fig. 3.2. Ripple in v_{ab} corresponding to the symmetric sequence of error vectors from Fig. 3.1.

1) We designate as $v_{e\alpha}$ and $v_{e\beta}$ the projections of the sequence of error vectors within a switching cycle on axis α and β, respectively. We will assume these two functions to be periodic with a period equal to T_s (this assumption is appropriate if the switching frequency is much higher than the output-voltage fundamental frequency [47]). We can then apply to both functions the Fourier transformation into a series of sinusoidal terms:

$$\begin{aligned} f(t) &= \frac{1}{2}\cdot a_0 + \sum_{n=1}^{\infty}\left(a_n\cdot\cos(n\omega_s t) + b_n\cdot\sin(n\omega_s t)\right) \\ a_n &= \frac{2}{T}\int_0^{T_s} f(t)\cdot\cos(n\omega_s t)\cdot dt, \quad n = 0,1,2,... \\ b_n &= \frac{2}{T}\int_0^{T_s} f(t)\cdot\sin(n\omega_s t)\cdot dt, \quad n = 1,2,... \end{aligned} \tag{3.2}$$

Since both $v_{e\alpha}$ and $v_{e\beta}$ have even symmetry, $b_n = 0$. The result of the Fourier transformation of both functions is then:

$$\begin{aligned} v_{e\alpha} &= \sum_n\left(a_{\alpha,n}\cdot\cos(n\omega_s t)\right) \\ v_{e\beta} &= \sum_n\left(a_{\beta,n}\cdot\cos(n\omega_s t)\right). \end{aligned} \tag{3.3}$$

2) For a given harmonic number n, the relationship

$$\cos(n\omega t) = \frac{e^{j\cdot n\omega t} + e^{-j\cdot n\omega t}}{2} \tag{3.4}$$

allows decomposing each of the harmonics of $v_{e\alpha}$ and $v_{e\beta}$ in (3.3) as the addition of two vectors rotating at frequency $n\cdot\omega_s$ in opposite directions:

$$\begin{aligned} v_{e\alpha} &= \sum_n \left(\frac{a_{\alpha,n}}{2}\cdot e^{j\cdot n\omega_s t} + \frac{a_{\alpha,n}}{2}\cdot e^{-j\cdot n\omega_s t} \right) = \sum_n \left(\mathbf{V}^+_{H\alpha n} + \mathbf{V}^-_{H\alpha n} \right) \\ j\cdot v_{e\beta} &= \sum_n \left(\frac{a_{\beta,n}}{2}\cdot e^{j\left(n\omega_s t+\frac{\pi}{2}\right)} + \frac{a_{\beta,n}}{2}\cdot e^{j\left(-n\omega_s t+\frac{\pi}{2}\right)} \right) = \sum_n \left(\mathbf{V}^+_{H\beta n} + \mathbf{V}^-_{H\beta n} \right). \end{aligned} \tag{3.5}$$

The four resulting rotating vectors ($\mathbf{V}^+_{H\alpha n}$, $\mathbf{V}^-_{H\alpha n}$, $\mathbf{V}^+_{H\beta n}$, $\mathbf{V}^-_{H\beta n}$) are represented in Fig. 3.3.

3) For a given harmonic number n, adding the vectors that rotate in the same direction, we obtain vectors $\mathbf{V}^+_{Hn}$ and $\mathbf{V}^-_{Hn}$ (Fig. 3.3):

$$\begin{aligned} \mathbf{V}^+_{Hn} &= \mathbf{V}^+_{H\alpha n} + \mathbf{V}^+_{H\beta n} = \frac{1}{2}\cdot\sqrt{a^2_{\alpha,n}+a^2_{\beta,n}}\cdot e^{j\left(n\omega_s t+\tan^{-1}\left(\frac{a_{\beta,n}}{a_{\alpha,n}}\right)\right)} \\ \mathbf{V}^-_{Hn} &= \mathbf{V}^-_{H\alpha n} + \mathbf{V}^-_{H\beta n} = \frac{1}{2}\cdot\sqrt{a^2_{\alpha,n}+a^2_{\beta,n}}\cdot e^{j\left(-n\omega_s t+\tan^{-1}\left(\frac{a_{\beta,n}}{a_{\alpha,n}}\right)\right)}. \end{aligned} \tag{3.6}$$

4) Finally, adding vectors $\mathbf{V}^+_{Hn}$ and $\mathbf{V}^-_{Hn}$, we obtain a single pulsating vector $\mathbf{V}_{Hn}$ (Fig. 3.3):

$$\mathbf{V}_{Hn} = \mathbf{V}^+_{Hn} + \mathbf{V}^-_{Hn} = \sqrt{a^2_{\alpha,n}+a^2_{\beta,n}}\cdot\cos(n\omega_s t)\cdot e^{j\cdot\tan^{-1}\left(\frac{a_{\beta,n}}{a_{\alpha,n}}\right)}. \tag{3.7}$$

The projection of $\mathbf{V}_{Hn}$ on any voltage axis determines the n^{th} harmonic of the corresponding voltage for a given switching cycle. The addition of all the series,

$$\mathbf{V}_H = \sum_{n=1}^{\infty}\mathbf{V}_{Hn} \tag{3.8}$$

defines a vector, $\mathbf{V}_H$, which, if projected on any voltage axis, determines the corresponding voltage ripple for a given switching cycle. Therefore, $\mathbf{V}_H$ is equivalent to the original sequence of $\mathbf{V}_e$.

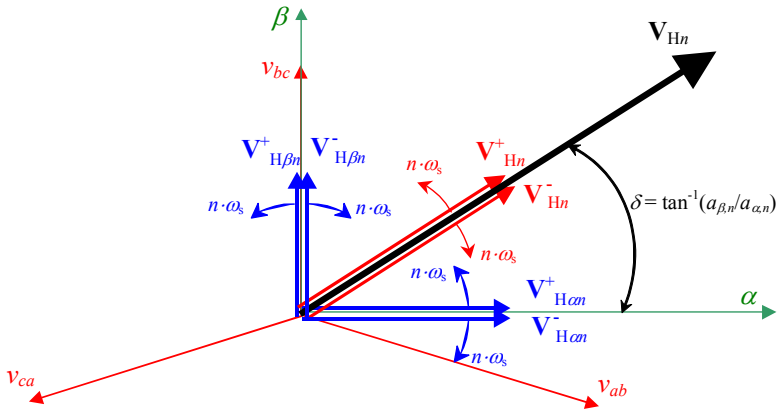


Fig. 3.3. Transformation of the sequence of error vectors into the addition of pulsating vectors $\mathbf{V}_{Hn}$.

3.2.3. Local and Global HD_n Definition

For the k^{th} switching cycle, the ripple at frequency $n{\cdot}f_s$ in the line-to-line and line-to-neutral voltages is

$$\begin{aligned}
V_{ab,n,k} &= V_{pn}\cdot\sqrt{a_{\alpha,n}^2+a_{\beta,n}^2}\cdot\left|\cos(\delta+\frac{\pi}{6})\right|\ [\mathrm{V_{pk}}], \quad V_{aN,n,k}=\frac{V_{pn}}{\sqrt{3}}\cdot\sqrt{a_{\alpha,n}^2+a_{\beta,n}^2}\cdot\left|\cos(\delta)\right|\ [\mathrm{V_{pk}}]\\
V_{bc,n,k} &= V_{pn}\cdot\sqrt{a_{\alpha,n}^2+a_{\beta,n}^2}\cdot\left|\cos(\frac{\pi}{2}-\delta)\right|\ [\mathrm{V_{pk}}], \quad V_{bN,n,k}=\frac{V_{pn}}{\sqrt{3}}\cdot\sqrt{a_{\alpha,n}^2+a_{\beta,n}^2}\cdot\left|\cos(\delta+\frac{\pi}{3})\right|\ [\mathrm{V_{pk}}] \qquad (3.9)\\
V_{ca,n,k} &= V_{pn}\cdot\sqrt{a_{\alpha,n}^2+a_{\beta,n}^2}\cdot\left|\cos(\delta-\frac{\pi}{6})\right|\ [\mathrm{V_{pk}}], \quad V_{cN,n,k}=\frac{V_{pn}}{\sqrt{3}}\cdot\sqrt{a_{\alpha,n}^2+a_{\beta,n}^2}\cdot\left|\cos(\delta-\frac{\pi}{3})\right|\ [\mathrm{V_{pk}}].
\end{aligned}$$

We can then define a single real number $HD_{n,k}$ that measures the per unit (p.u.) local distortion in the output three-phase voltage as

$$HD_{n,k}=\frac{1}{m\cdot V_{pn}}\cdot\sqrt{\frac{1}{3}\cdot\left(V_{ab,n,k}^2+V_{bc,n,k}^2+V_{ca,n,k}^2\right)}=\frac{\sqrt{3}}{m\cdot V_{pn}}\cdot\sqrt{\frac{1}{3}\cdot\left(V_{aN,n,k}^2+V_{bN,n,k}^2+V_{cN,n,k}^2\right)}\ [\mathrm{p.u.}] \qquad (3.10)$$

where m is the modulation index ($m \in [0, 1]$). Substituting (3.9) in (3.10) and simplifying

$$HD_{n,k}=\frac{1}{m}\cdot\sqrt{\frac{a_{\alpha,n}^2+a_{\beta,n}^2}{2}}\ \ [\mathrm{p.u.}]. \qquad (3.11)$$

For a whole output-voltage line cycle, we can define a single real number HD_n that measures the global distortion in the output three-phase voltage at around frequency $n{\cdot}f_s$ by analyzing the local distortion $HD_{n,k}$ within the first sextant of the SVD and then calculating

$$HD_n=\sqrt{\frac{1}{K_T}\cdot\sum_{k=1}^{K_T}HD_{n,k}^2}\ \ [\mathrm{p.u.}] \qquad (3.12)$$

where K_T is the total number of switching cycles within the first sextant of the SVD. Define the rms output-voltage distortion in the line-to-line (V^{Δ}_{dis}) and line-to-neutral (V^{Y}_{dis}) voltages at around $n{\cdot}f_s$ as

$$\begin{aligned}
V_{\text{dis},n}^{\Delta} &= \sqrt{\sum_{(n-0.5)\cdot f_s/f_o\le h<(n+0.5)\cdot f_s/f_o}\left(V_h^{\Delta}\right)^2}\ \ [\mathrm{V_{rms}}]\\
V_{\text{dis},n}^{\mathrm{Y}} &= \sqrt{\sum_{(n-0.5)\cdot f_s/f_o\le h<(n+0.5)\cdot f_s/f_o}\left(V_h^{\mathrm{Y}}\right)^2}\ \ [\mathrm{V_{rms}}]
\end{aligned} \qquad (3.13)$$

where V_h^{Δ} and V_h^{Y} are the rms value of the h^{th} harmonic of the output line-to-line and line-to-neutral voltages, respectively, and f_o is the fundamental frequency. We can easily calculate this distortion from the value of HD_n as

$$V_{\text{dis},n}^{\Delta} = m \cdot \frac{V_{pn}}{\sqrt{2}} \cdot HD_n \left[\text{V}_{\text{rms}}\right]$$
$$V_{\text{dis},n}^{\text{Y}} = m \cdot \frac{V_{pn}}{\sqrt{6}} \cdot HD_n \left[\text{V}_{\text{rms}}\right]. \tag{3.14}$$

Hence, the total harmonic distortion for both line-to-line and line-to-neutral voltages can be calculated as

$$THD = \sqrt{\sum_n HD_n^2} \cdot 100 \ [\%]. \tag{3.15}$$

It is interesting to note that the *THD* is the same for both line-to-line and line-to-neutral voltages even though the projection of the 3L-3P NPC VSI voltage space vectors defines nine possible voltage levels in the line-to-neutral voltages, whereas it defines only five in the line-to-line voltages (see Fig. 3.1).

3.3. Expression of HD_n for the 3L-3P NPC VSI

Let us assume that in the first sextant of the SVD for the 3L-3P NPC VSI any of the ten possible switching states can be selected. Let us also assume that the first half of the selected symmetric sequence of switching states is: *ppp*, *ppo*, *ppn*, *poo*, *pon*, *pnn*, *ooo*, *oon*, *onn*, *nnn*. Then, in the first sextant of the normalized SVD, the expression for $a_{\alpha,n}$ and $a_{\beta,n}$ is

$$a_{\alpha,n} = \frac{1}{\sqrt{3} \cdot n \cdot \pi} \cdot \left[-E1 - E2 - E4 - E5 + (-1)^n \cdot (-4 \cdot E6 + E7 + E8 - 2 \cdot E9) \right]$$
$$a_{\beta,n} = \frac{1}{n \cdot \pi} \cdot \left[-E1 - E2 + 2 \cdot E3 - E4 + E5 + (-1)^n \cdot (E7 - E8) \right]$$

$$\begin{aligned}
E1 &= \sin(n \cdot \pi \cdot d_{ppp}) \\
E2 &= \sin\left[n \cdot \pi \cdot (d_{ppp} + d_{ppo})\right] \\
E3 &= \sin\left[n \cdot \pi \cdot (d_{ppp} + d_{ppo} + d_{ppn})\right] \\
E4 &= \sin\left[n \cdot \pi \cdot (d_{ppp} + d_{ppo} + d_{ppn} + d_{poo})\right] \\
E5 &= \sin\left[n \cdot \pi \cdot (d_{ppp} + d_{ppo} + d_{ppn} + d_{poo} + d_{pon})\right] \\
E6 &= \sin\left[n \cdot \pi \cdot (d_{nnn} + d_{onn} + d_{oon} + d_{ooo})\right] \\
E7 &= \sin\left[n \cdot \pi \cdot (d_{nnn} + d_{onn} + d_{oon})\right] \\
E8 &= \sin\left[n \cdot \pi \cdot (d_{nnn} + d_{onn})\right] \\
E9 &= \sin(n \cdot \pi \cdot d_{nnn})
\end{aligned} \tag{3.16}$$

where d_{xyz} is the duty ratio of switching state *xyz*.

These expressions are valid for most of the modulation strategies proposed in the literature. In particular, they are valid for any NTV PWM with the sequence of switching states selected in

order to minimize the number of commutations. Using (3.16) and (3.11) we obtain the value of $HD_{n,k}$. Then, using (3.12) we obtain the value of HD_n.

3.4. Comparison of HD_n Predictions with FFT-Based Results

Fig. 3.4 shows the calculated $HD_{n,k}$ (n = 1, 2) for the NTV50 PWM.

The resulting values of $V^{\Delta}_{\text{dis},1}$, $V^{\Delta}_{\text{dis},2}$, $V^{\Delta}_{\text{dis},3}$, and $V^{\Delta}_{\text{dis},4}$ after applying (3.12) and (3.14) are presented in Table 3.1 (V_{pn} = 150 V). It can be seen that the distortion levels calculated through HD_n are fairly close to the distortion levels calculated applying the FFT to v_{ab} for one line cycle and then using (3.13). Fig. 3.5 presents the simulated and experimental v_{ab} and FFT(v_{ab}) waveforms.

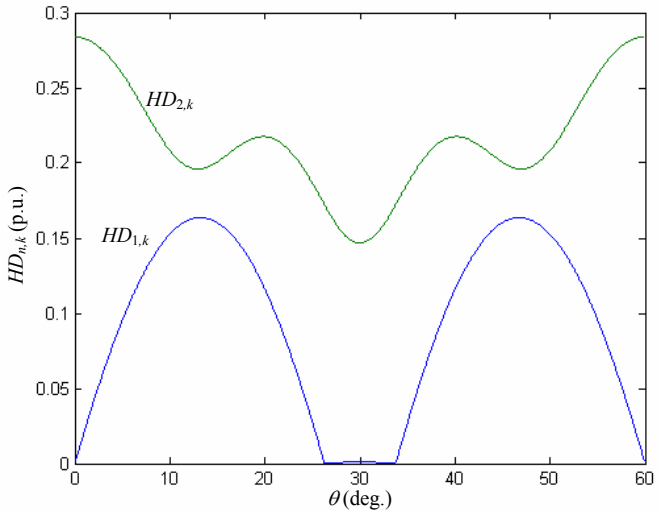
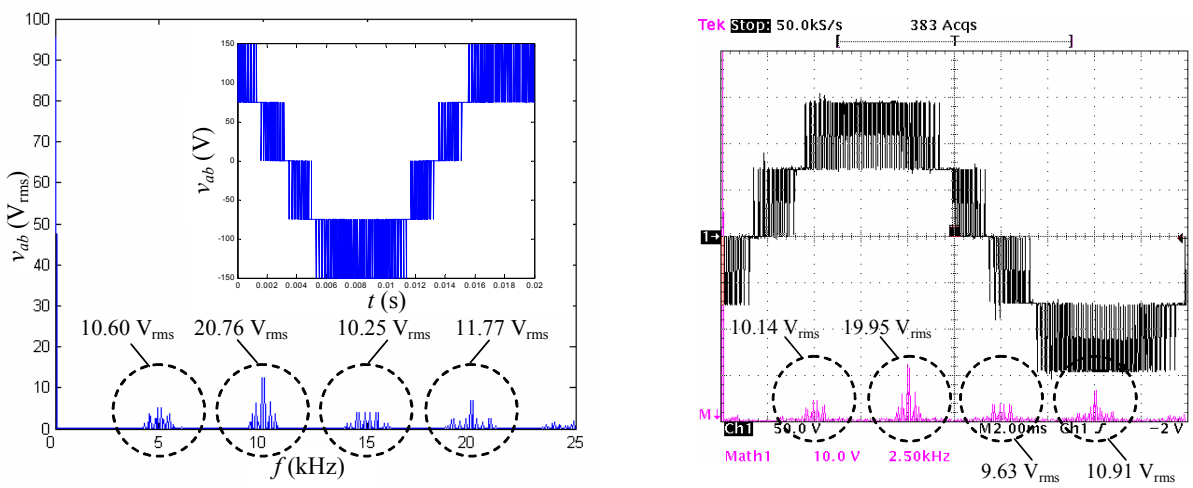


Fig. 3.4. Calculated $HD_{n,k}$ (n = 1, 2) as a function of the $\mathbf{V}_{\text{ref}}$'s angle θ at which switching cycle k is centered, for the NTV50 PWM (m = 0.9).

Computation method	$V^{\Delta}_{\text{dis},1}$ [V_{rms}]	$V^{\Delta}_{\text{dis},2}$ [V_{rms}]	$V^{\Delta}_{\text{dis},3}$ [V_{rms}]	$V^{\Delta}_{\text{dis},4}$ [V_{rms}]
A. Equations (3.16) + (3.11) + (3.12) + (3.14)	10.40	20.91	10.14	11.65
B. FFT(v_{ab})* from simulation + (3.13)	10.60	20.76	10.25	11.77
C. FFT(v_{ab})* from experiment + (3.13)	10.14	19.95	9.63	10.91

Table 3.1. Comparison of $V^{\Delta}_{\text{dis},n}$ values obtained from the computation of HD_n with those obtained from FFT-based results from simulation and experiments.

* Sampling frequency = 409.6 kHz.



(a) *(b)*

Fig. 3.5. v_{ab} *[50 V/div] and* FFT(v_{ab}) *[10* V_{rms}*/div] for the NTV50 PWM (*V_{pn} *= 150 V,* m *= 0.9). (a) Simulated. (b) Experimental.*

Given all the switching-state duty-ratios in the first sextant of the SVD, the computation of $V^{\Delta}_{\text{dis},n}$ up to $n = 4$ takes 12.6 ms for Method A, while it takes 770 ms for Method B (MATLAB 6.0, Intel Pentium III @ 450 MHz). The lower computational effort required with Method A is mainly due to the a priori application in (3.16) of the Fourier series decomposition to the known square-wave type voltage waveforms. Furthermore, the results obtained applying the FFT are approximate. Increasing the number of samples used to perform the FFT increases the accuracy, but it also increases the computational effort required. Last, as the order n of the distortion being analyzed increases, the sampling frequency must also increase to guarantee a certain degree of accuracy, increasing the number of computations. Instead, in Method A, the computational effort to obtain $V_{\text{dis},n}$ is always the same regardless of the order n.

3.5. Conclusions

This chapter has presented a novel figure, $HD_{n,k}$, allowing us to quantitatively characterize the output three-phase voltage distortion at around $n{\cdot}f_s$ per switching-cycle k. The expression of $HD_{n,k}$ as a function of the switching state duty-ratios has been derived for the 3L-3P NPC VSI and it can be easily obtained for any other multilevel converter.

From the evaluation of $HD_{n,k}$ over $1/6^{\text{th}}$ of the output-voltage fundamental cycle, the value of HD_n is calculated, providing a measure of the output-voltage distortion in a fundamental cycle. This information is obtained at a lower computational cost than through conventional FFT analysis.

The distortion predictions of HD_n are accurate, as has been verified by comparing them to FFT-based results obtained from simulation and experiments. The value of *THD* can also be calculated from the values of HD_n using (3.15).

From (3.12), and since $HD_{n,k} \geq 0$, we can conclude that to minimize HD_n we only need to minimize $HD_{n,k}$ for all switching cycles within one sextant of the SVD. This allows decomposing the modulation design problem within an output-voltage fundamental cycle into an independent set of smaller problems for every switching cycle. Through the expression of $HD_{n,k}$, the voltage distortion around multiples of the switching frequency is easily incorporated as a design parameter in the process of defining PWM strategies for multilevel converters, and the search for optimum modulations from the point of view of voltage distortion is simplified.

CHAPTER 4

OPTIMIZED NEAREST-THREE VIRTUAL-SPACE-VECTOR PULSEWIDTH MODULATION

Abstract — This chapter presents a new modulation approach for the complete control of the neutral-point voltage in the three-level three-phase neutral-point-clamped voltage source inverter. The dc-link voltage balancing is achieved over the full range of converter output voltages and for all load power factors with the minimum output-voltage distortion at around the switching frequency. The simple phase duty-ratio expressions in d-q-0 coordinates that define this modulation are presented. The performance of this modulation approach and its benefits over other previously proposed solutions are verified through simulation and experiments.

4.1. Introduction

The NTV^2 PWM proposed in Chapter 2 allows controlling the neutral-point voltage over the full range of converter output voltage and for any load (linear or not), provided that the addition of the three output phase currents equals zero. But, in the case of a linear and balanced load, the distortion of the output voltage around the switching frequency is higher than needed to achieve this goal. This has been demonstrated in Section 2.6, where the NTV^2 PWM performance was compared to the performance of the Song PWM. In the case of a linear and balanced load, the Song PWM is capable of controlling the neutral-point voltage with a lower (not minimum) output-voltage switching-frequency distortion and lower number of commutations, but only over a limited range of output voltage amplitudes for each load power factor.

In this chapter, and starting from the NTV^2 PWM, a new modulation solution is derived to comprehensively control the neutral-point voltage, for any load, and with the minimum output-voltage distortion at around the switching frequency.

The chapter is organized as follows. In Section 4.2, the proposed modulation is presented. Sections 4.3 and 4.4 depict the simulation and experimental results comparing the proposed modulation to previous solutions, and the chapter is concluded in Section 4.5.

4.2. Optimized Nearest-Three Virtual-Space-Vector PWM

In [48], the state-space model of the system in Fig. 1.2(a) in both *a-b-c* and *d-q-0* coordinates is presented. The model has six independent control variables:

a) In *a-b-c* coordinates, these are d_{ap}, d_{bp}, d_{cp}, d_{an}, d_{bn}, d_{cn}, where d_{xy} is the duty ratio of the phase x connection to the dc-link point y.

b) In *d-q-0* coordinates, these are d_{pd}, d_{pq}, d_{p0}, d_{nd}, d_{nq}, d_{n0}, which correspond to the *d-q-0* transformation of the positive and negative phase duty-ratios in *a-b-c* coordinates as expressed in

$$\begin{bmatrix} d_{pd} & d_{nd} \\ d_{pq} & d_{nq} \\ d_{p0} & d_{n0} \end{bmatrix} = [T] \cdot \begin{bmatrix} d_{ap} & d_{an} \\ d_{bp} & d_{bn} \\ d_{cp} & d_{cn} \end{bmatrix}$$

$$[T] = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos(\omega_o t) & \cos(\omega_o t - 2\pi/3) & \cos(\omega_o t + 2\pi/3) \\ -\sin(\omega_o t) & -\sin(\omega_o t - 2\pi/3) & -\sin(\omega_o t + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}. \tag{4.1}$$

In the following, the equations that define the duty-ratio pattern of the proposed PWM are presented. They are derived for the system in Fig. 1.2(a), assuming a linear and balanced load with power factor equal to cos(φ), identical dc-link capacitors ($C_1 = C_2 = C_{dc}$), switching frequency significantly higher than the output-voltage fundamental frequency, and the symmetrical sequence, within a switching cycle, of connection of each phase to each of the dc-bus points: *p-o-n-o-p* (Fig. 2.2.)

In order to derive the proposed modulation, let us first consider a generalization of the NTV[2] PWM. Fig. 4.1 shows the normalized general VVs for the first sextant of the 3L-3P NPC VSI SVD.

As shown in Fig. 4.1, the general virtual space vectors $\mathbf{V}_{G0}$, $\mathbf{V}_{GSi}$, $\mathbf{V}_{GMi}$, and $\mathbf{V}_{GLi}$ (i = 1, 2…6) are defined as a linear combination of the real converter space vectors $\mathbf{V}_0$, $\mathbf{V}_{Si}$, $\mathbf{V}_{Mi}$, and $\mathbf{V}_{Li}$, associated to certain switching states. The coefficients of the linear combination are the seven unknowns: $r_1 - r_7$. In every switching cycle, the rotating reference vector $\mathbf{V}_{ref}$ is synthesized using

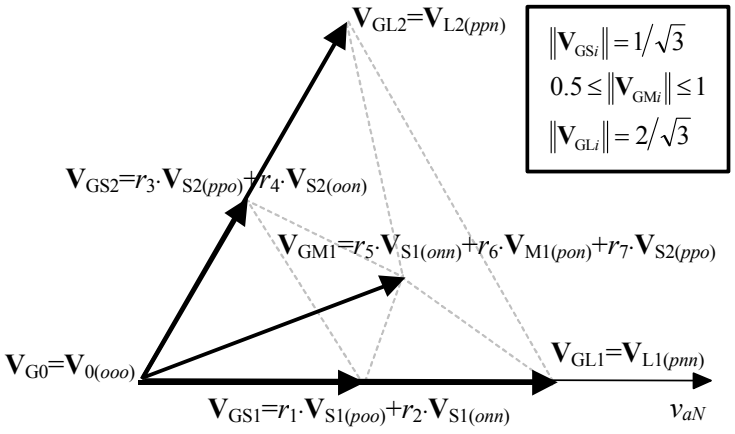


Fig. 4.1. Normalized general VVs for the first sextant of the SVD.

the nearest-three general VVs. Using analogous equations as those presented in Chapter 2, the VVs' duty-ratios are initially calculated. From this information, all the switching state duty-ratios are calculated. Finally, from these, $d_{ap}, d_{bp}, d_{cp}, d_{an}, d_{bn}, d_{cn}$ are obtained.

The SVD in Fig. 4.1 is general in the sense that it includes the most common modulation strategies presented in the literature. For instance, if $r_5, r_7 = 0$, the traditional NTV PWM family is obtained. If $r_1, r_2, r_3, r_4 = 1/2$ and $r_5, r_6, r_7 = 1/3$, we obtain the NTV^2 PWM.

The objective here is to find the set of values $r_{1,k} - r_{7,k}$ for every switching cycle k within a line cycle that minimizes the output-voltage distortion around f_s, $V_{\text{dis},1}$ ($V^{\Delta}_{\text{dis},1}$ or $V^{Y}_{\text{dis},1}$) (3.13), while guaranteeing a zero average i_o in every switching cycle. Due to the six-fold symmetry of the SVD, we only need to find the values of $r_{1,k} - r_{7,k}$ within the first sextant. As explained in Chapter 3, in order to minimize $V_{\text{dis},1}$ we just need to minimize the per switching-cycle k figure $HD_{1,k}$ for all switching cycles within the first sextant. Hence, for a given modulation index m and load angle φ, a per switching-cycle optimization problem can be formulated with the objective function to minimize being

$$f\left(r_{1,k}, r_{2,k} \ldots r_{7,k}\right) = HD_{1,k}\left(r_{1,k}, r_{2,k} \ldots r_{7,k}\right) \tag{4.2}$$

and with constraints

$$\begin{gathered} \int_{(k-1)\cdot T_s}^{k\cdot T_s} i_o\left(r_{1,k}, r_{2,k} \ldots r_{7,k}\right)\cdot dt = 0, \qquad r_{1,k}, r_{2,k} \ldots r_{7,k} \geq 0 \\ r_{1,k} + r_{2,k} = 1, \quad r_{3,k} + r_{4,k} = 1, \quad r_{5,k} + r_{6,k} + r_{7,k} = 1. \end{gathered} \tag{4.3}$$

The optimization problem stated in (4.2) and (4.3) was solved employing MATLAB's Optimization Toolbox. Fig. 4.2 shows the resulting optimum d_{ap} and d_{an} waveforms for a whole line cycle, $m = 0.7$, and $\varphi = 30º$, 0º, and -30º. The duty ratios for phases b and c are the same but phase-shifted ±120º. Fig. 4.3 presents the corresponding duty ratios in *d-q-0* coordinates. These last duty ratios present a pattern that can be expressed mathematically with the following six equations:

$$\begin{aligned} d_{pd} &= \tan(\varphi)\cdot d_{pq} + m/\sqrt{2} \\ d_{nd} &= d_{pd} - \sqrt{2}\cdot m \\ d_{nq} &= d_{pq} \end{aligned} \tag{4.4}$$

$$\begin{cases} \theta \leq 2\pi/3: \;\; d_{p0} = \sqrt{2}\cdot\left(-d_{pd}\cdot\cos(\theta + 2\pi/3) + d_{pq}\cdot\sin(\theta + 2\pi/3)\right) \\ 2\pi/3 < \;\theta \leq 4\pi/3: \;\; d_{p0} = \sqrt{2}\cdot\left(-d_{pd}\cdot\cos(\theta) + d_{pq}\cdot\sin(\theta)\right) \\ \theta > 4\pi/3: \;\; d_{p0} = \sqrt{2}\cdot\left(-d_{pd}\cdot\cos(\theta - 2\pi/3) + d_{pq}\cdot\sin(\theta - 2\pi/3)\right) \end{cases} \tag{4.5}$$

$$\begin{cases} \theta \le \pi/3,\ \theta > 5\pi/3: \ \ d_{n0} = \sqrt{2}\cdot\left(-d_{nd}\cdot\cos(\theta)+d_{nq}\cdot\sin(\theta)\right) \\ \pi/3 < \theta \le \pi: \ \ d_{n0} = \sqrt{2}\cdot\left(-d_{nd}\cdot\cos(\theta-2\pi/3)+d_{nq}\cdot\sin(\theta-2\pi/3)\right) \\ \pi < \theta \le 5\pi/3: \ \ d_{n0} = \sqrt{2}\cdot\left(-d_{nd}\cdot\cos(\theta+2\pi/3)+d_{nq}\cdot\sin(\theta+2\pi/3)\right) \end{cases} \tag{4.6}$$

$$d_{pq} = -K\cdot\sin(3\theta). \tag{4.7}$$

The three equations in (4.4) can be obtained by solving in steady state the system of equations in (4.8) [48], corresponding to the model of the system in *d-q-0* coordinates, where i_d, i_q and $v^{\mathrm{Y}}{}_d$, $v^{\mathrm{Y}}{}_q$ are the *d-q* components of the line currents and line-to-neutral resistor R_{L} voltages, respectively (Fig. 1.2(a).) The three equations in (4.4) guarantee steady state for the output voltages

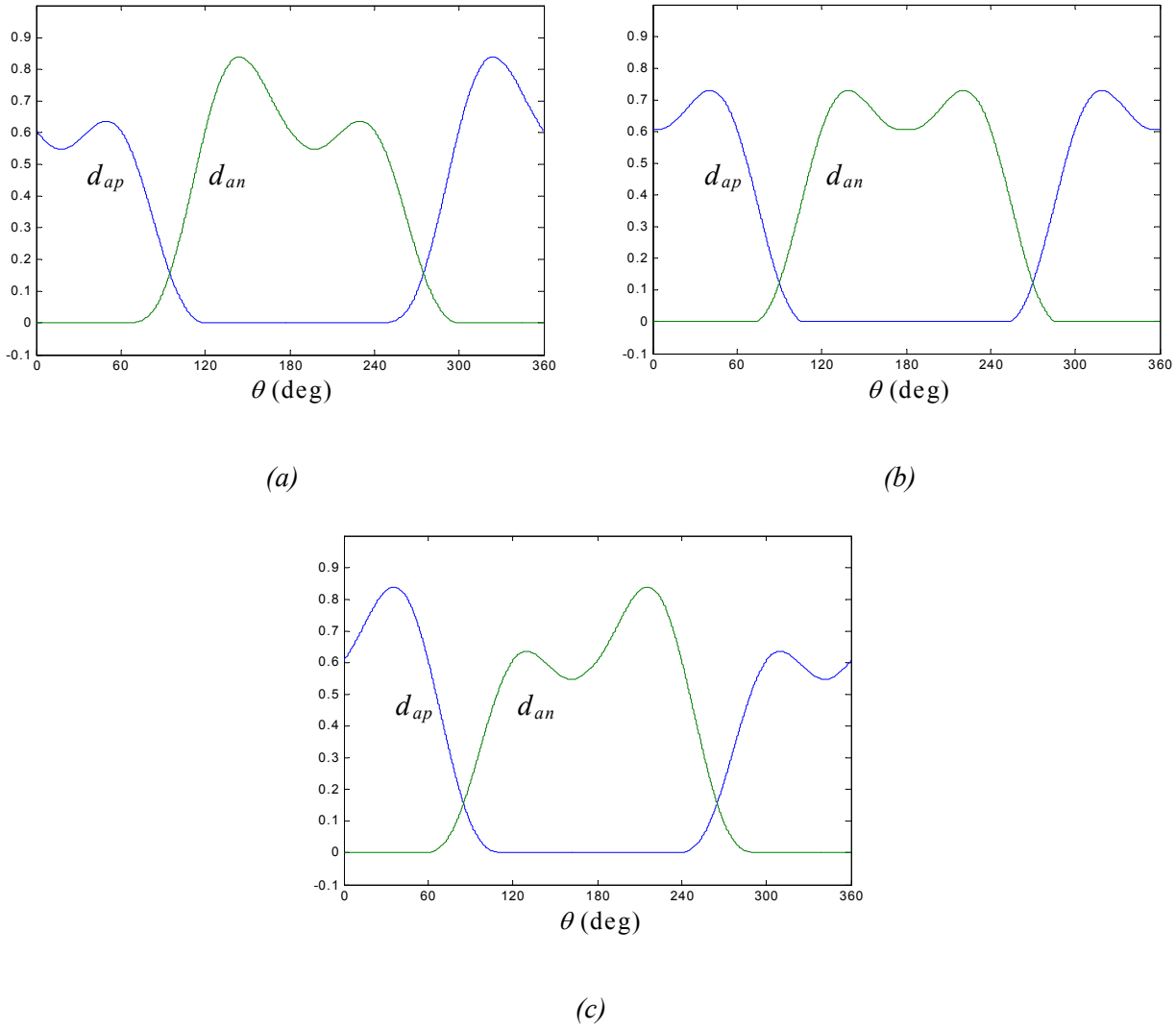
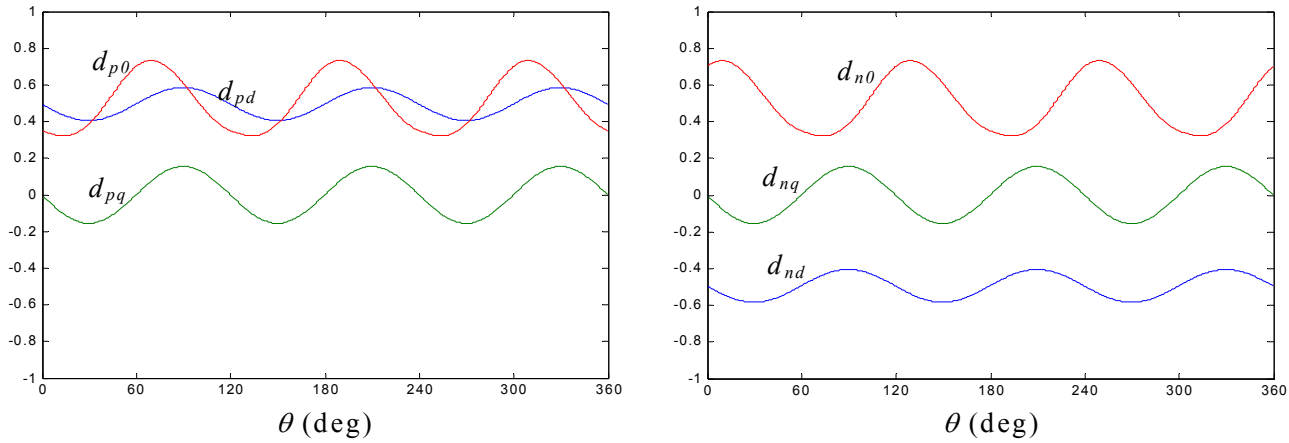
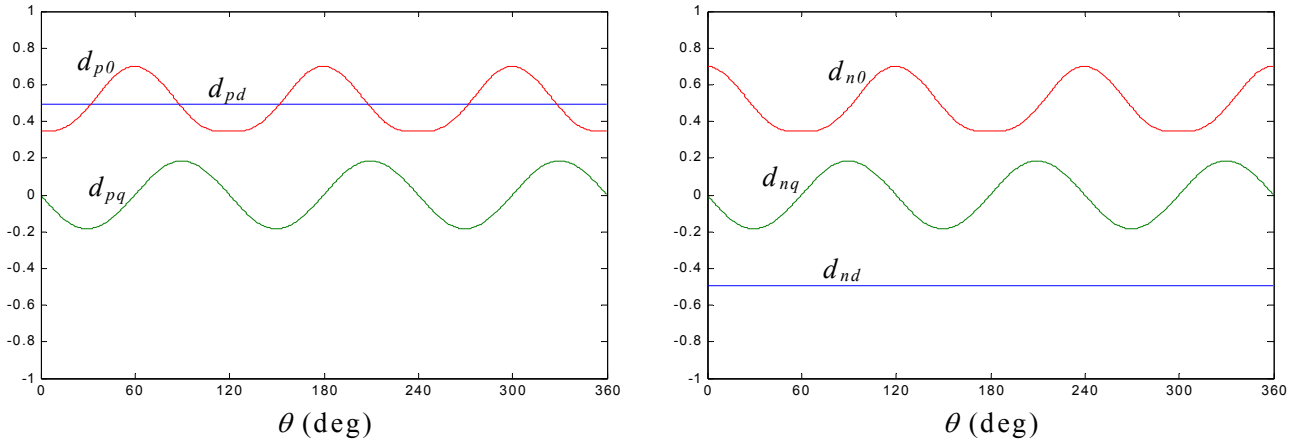


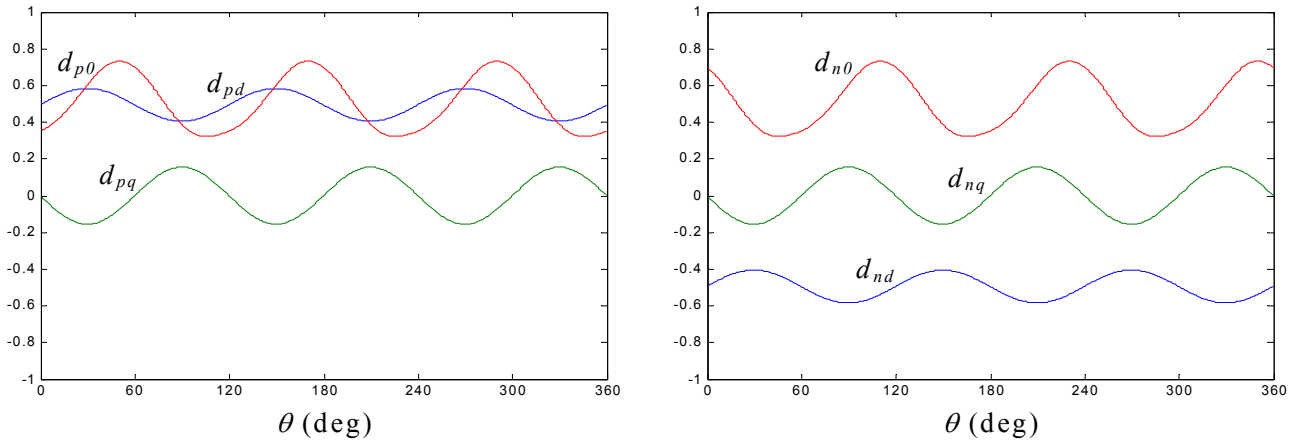
Fig. 4.2. Optimum d_{ap} and d_{an} waveforms as a function of θ for m = 0.7 and (a) φ = 30º, (b) φ = 0º, (c) φ = -30º.



(a)



(b)



(c)

Fig. 4.3. Optimum d_{pd}, d_{pq}, d_{p0}, d_{nd}, d_{nq}, and d_{n0} waveforms as a function of θ for m = 0.7 and (a) φ = 30°, (b) φ = 0°, (c) φ = -30°.

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ v_d^{\mathrm{Y}} \\ v_q^{\mathrm{Y}} \\ v_{C1} \\ v_{C2} \end{bmatrix} = \begin{bmatrix} 0 & \omega_{\mathrm{o}} & -1/L_{\mathrm{L}} & 0 & d_{pd}/L_{\mathrm{L}} & -d_{nd}/L_{\mathrm{L}} \\ -\omega_{\mathrm{o}} & 0 & 0 & -1/L_{\mathrm{L}} & d_{pq}/L_{\mathrm{L}} & -d_{nq}/L_{\mathrm{L}} \\ 1/C_{\mathrm{L}} & 0 & -1/R_{\mathrm{L}}C_{\mathrm{L}} & \omega_{\mathrm{o}} & 0 & 0 \\ 0 & 1/C_{\mathrm{L}} & -\omega_{\mathrm{o}} & -1/R_{\mathrm{L}}C_{\mathrm{L}} & 0 & 0 \\ -d_{pd}/C_{\mathrm{dc}} & -d_{pq}/C_{\mathrm{dc}} & 0 & 0 & 0 & 0 \\ d_{nd}/C_{\mathrm{dc}} & d_{nq}/C_{\mathrm{dc}} & 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \\ v_d^{\mathrm{Y}} \\ v_q^{\mathrm{Y}} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 1/C_{\mathrm{dc}} \\ 1/C_{\mathrm{dc}} \end{bmatrix} \cdot I. \qquad (4.8)$$

and currents and no low-frequency variation of the neutral-point voltage. Hence, any modulation strategy that aims to control the neutral-point voltage should verify these three equations.

Equations (4.5) and (4.6) express the fact that in the optimum modulation solution each of the phase duty-ratios d_{ap}, d_{bp}, d_{cp}, d_{an}, d_{bn}, and d_{cn} is equal to zero over 120º of the output-voltage fundamental cycle.

Finally, (4.7) is introduced after observing that, in the optimum solution, duty ratio d_{pq} approximately follows a sinusoidal pattern at a frequency equal to $3 \cdot f_{\mathrm{o}}$.

The amplitude K in (4.7) must have a value within [0, $K_{\max}$], where $K_{\max}$ is the value above which d_{ap}, d_{an}, etc. reach values outside [0, 1]. Table 4.1 shows $K_{\max}$ (first entry in each cell) for different pairs of values of m and φ. The optimum value of K (K_{opt}) for every m and φ can be obtained through solving the optimization problem or by simple iteration and analysis of $V_{\mathrm{dis},1}$. These optimum values (third entry) and their corresponding value of HD_1 (fourth entry) has also been included in Table 4.1. Finally, the table is completed with the range of values for K (second entry in each cell) that lead to a distortion $V_{\mathrm{dis},1}$ lower than 1.01 times the distortion for K_{opt}.

It is convenient to have an expression of K_{opt} as a function of m and φ. With this aim, the m-φ operating plane in Fig. 4.4 is divided into three regions: A, B, and C. The expressions defining the boundaries in between regions are

$$\begin{aligned} m_{\mathrm{b_{AB}}} &= 0.5 \\ m_{\mathrm{b_{BC}}} &= 0.75 + 0.213 \cdot \left[1 - \sin\left(|\varphi|\right)\right]. \end{aligned} \qquad (4.9)$$

In regions A, B, and C, K_{opt} can be approximated by the expressions K_{A}, K_{B}, and K_{C}, in (4.10). These expressions provide an estimation of the optimum value of K within the ranges specified in Table 4.1. Hence, they lead to a distortion $V_{\mathrm{dis},1}$ lower than 1.01 times the distortion for the tabulated value of K_{opt}.

K_{max} (x10^{-3}) [K_{opt_min}, K_{opt_max}] (x10^{-3}) K_{opt} (x10^{-3}) HD_{1_opt} (x10^{-2})	$\varphi = 0º$	$\varphi = \pm 20º$	$\varphi = \pm 40º$	$\varphi = \pm 60º$	$\varphi = \pm 80º$	$\varphi = \pm 90º$
$m = 0.98$	160 [138,160] 160 29.4	35 [0,35] 35 35.6	16 [0,16] 15 36.1	8 [0,8] 6 36.2	3 [0,3] 3 36.2	0 [0,0] 0 36.4
$m = 0.95$	250 [230,250] 250 20.1	90 [60,90] 90 32.4	45 [0,45] 45 34.5	20 [0,20] 20 35.3	10 [0,10] 10 35.4	0 [0,0] 0 35.5
$m = 0.90$	240 [222,240] 240 16.8	170 [148,170] 170 24.7	85 [35,85] 85 31.4	45 [0,45] 30 33.6	15 [0,15] 5 33.9	0 [0,0] 0 34.0
$m = 0.80$	215 [194,215] 215 10.1	205 [172,205] 205 14.9	165 [80,165] 160 23.8	85 [0,85] 30 29.0	25 [0,15] 5 30.1	0 [0,0] 0 30.4
$m = 0.70$	190 [155,190] 185 4.5	180 [140,180] 170 8.5	165 [90,165] 140 15.7	125 [10,110] 60 22.8	40 [0,20] 5 25.4	0 [0,0] 0 25.6
$m = 0.60$	165 [100,138] 120 2.2	155 [95,145] 120 3.7	140 [82,140] 120 7.0	115 [42,115] 100 13.4	50 [0,28] 10 19.8	0 [0,0] 0 20.5
$m = 0.50$	140 [5,85] 70 1.8	135 [52,87] 70 2.0	120 [50,92] 70 2.4	100 [45,100] 75 4.5	50 [0,38] 15 13.6	0 [0,0] 0 15.2
$m = 0.40$	115 [15,55] 35 2.4	110 [17,53] 35 2.7	100 [12,52] 30 4.0	80 [0,45] 25 6.4	40 [0,15] 5 9.7	0 [0,0] 0 10.5
$m = 0.30$	89 [0,30] 15 2.9	83 [0,32] 14 3.2	74 [0,25] 11 3.9	60 [0,19] 5 5.3	31 [0,5] 0 6.3	0 [0,0] 0 6.3
$m = 0.20$	64 [0,20] 4 3.8	59 [0,18] 4 4.1	52 [0,16] 2 4.5	42 [0,10] 1 4.5	21 [0,3] 0 4.7	0 [0,0] 0 4.7
$m = 0.10$	37 [0,15] 0 6.9	33 [0,13] 0 6.9	29 [0,12] 0 6.9	24 [0,7] 0 6.9	12 [0,2] 0 6.9	0 [0,0] 0 6.9

Table 4.1. K_{max}, K_{opt_min}, K_{opt_max}, K_{opt} *and* HD_{1_opt} *for different values of m and* φ.

Non-shaded cells: region A. *Light-grey shaded cells: region* B. *Dark-grey shaded cells: region* C.

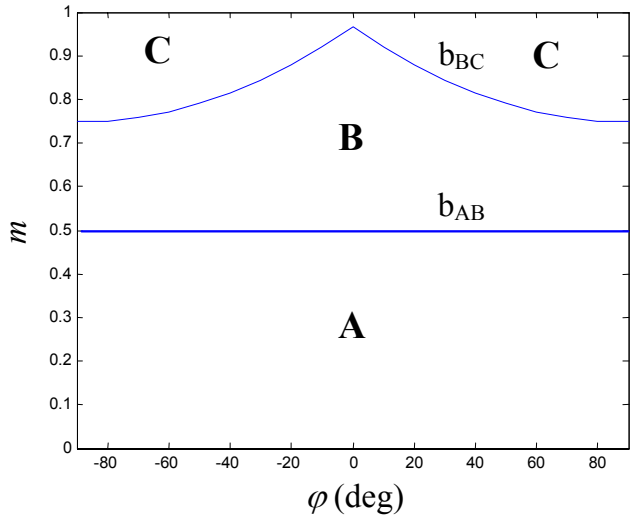


Fig. 4.4. Regions A, B, *and* C *for the approximation of* K_{opt}.

$$K_A = 0.25 \cdot m^2 \cdot \cos(\varphi)$$

$$K_B = 0.25 \cdot m \cdot \left(1 - \frac{|\varphi|}{\pi/2}\right) \tag{4.10}$$

$$K_C = \frac{1.53 \cdot (1-m) \cdot \left[1 - \sin(|\varphi|)\right]}{(|\varphi| + 0.24)}.$$

It is interesting to note that for the two cases: $m = 1$ and $|\varphi| = 90º$, $K_{opt} = 0$, and in this particular case, the optimum modulation solution defined by (4.4)–(4.7) is equivalent to the NTV^2 PWM. The optimum value of K will also be zero under unbalanced or non-linear loads, since this is the only value that guarantees the dc-link voltage balancing. Hence, the proposed modulation, designated as the optimized nearest-three virtual-space-vector (ONTV^2) PWM, is in fact a generalization of the NTV^2 PWM. It can also be used for any load (linear or nonlinear) achieving full control of the neutral-point voltage, but now allowing a better high-frequency harmonic distortion content under linear and balanced loads.

4.3. Simulation Results

4.3.1. ONTV^2 vs. NTV^2

In Fig. 4.5, the ONTV^2 PWM is compared to the NTV^2 PWM under a linear and balanced load. In both modulations, the average i_o in each switching cycle is zero. Hence, there is no low-frequency oscillation of the neutral-point voltage. However, the modulation proposed in this

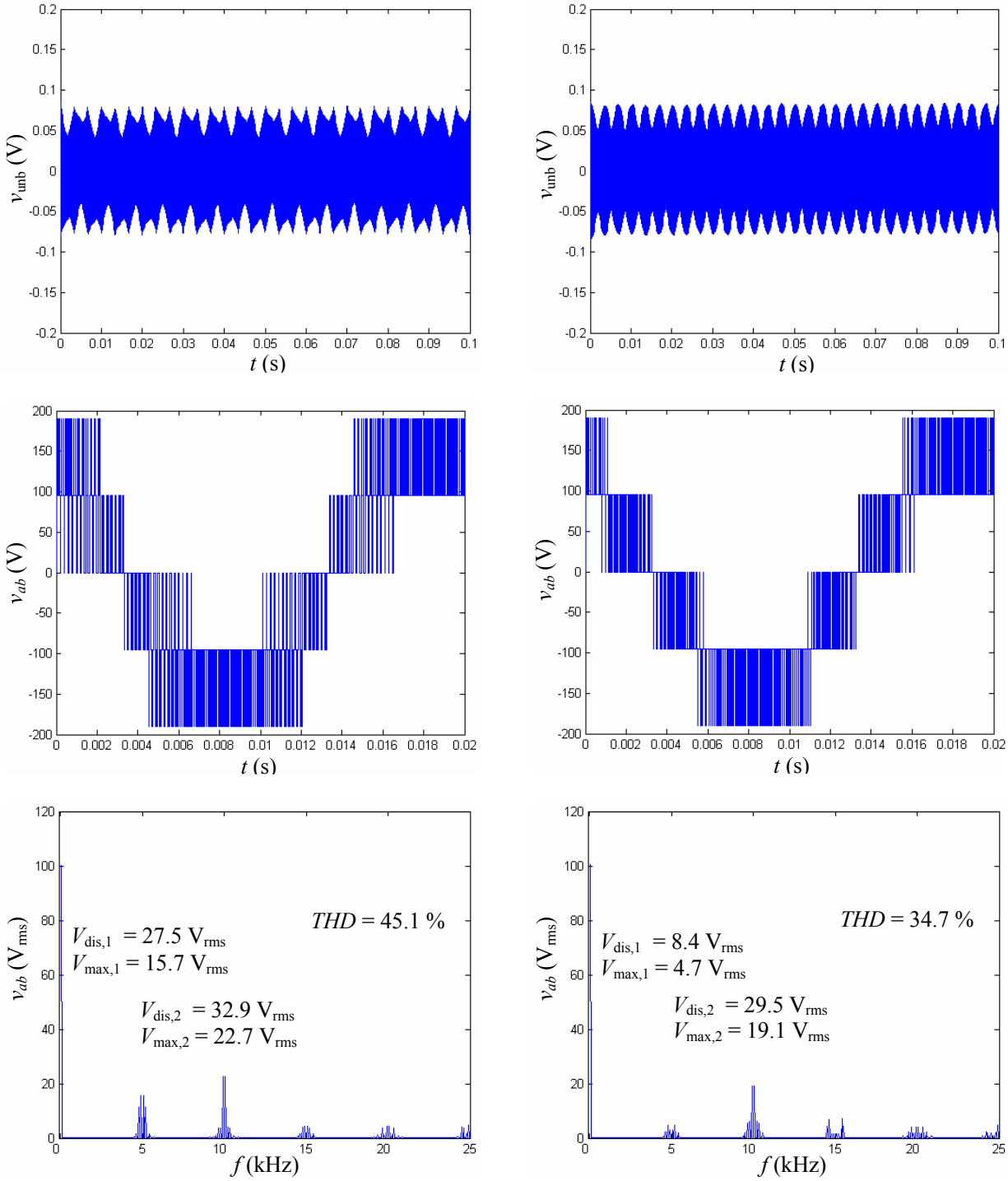


Fig. 4.5. Simulation results for v_{unb}, output voltage v_{ab}, and FFT(v_{ab}) *in the conditions: V_{pn} = 190 V, m = 0.75, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 1.1 mF, R_L = 16.5 Ω, C_L = 0 F, and L_L = 5 mH (φ = 5.44°). (a) NTV² PWM. (b) ONTV² PWM.*

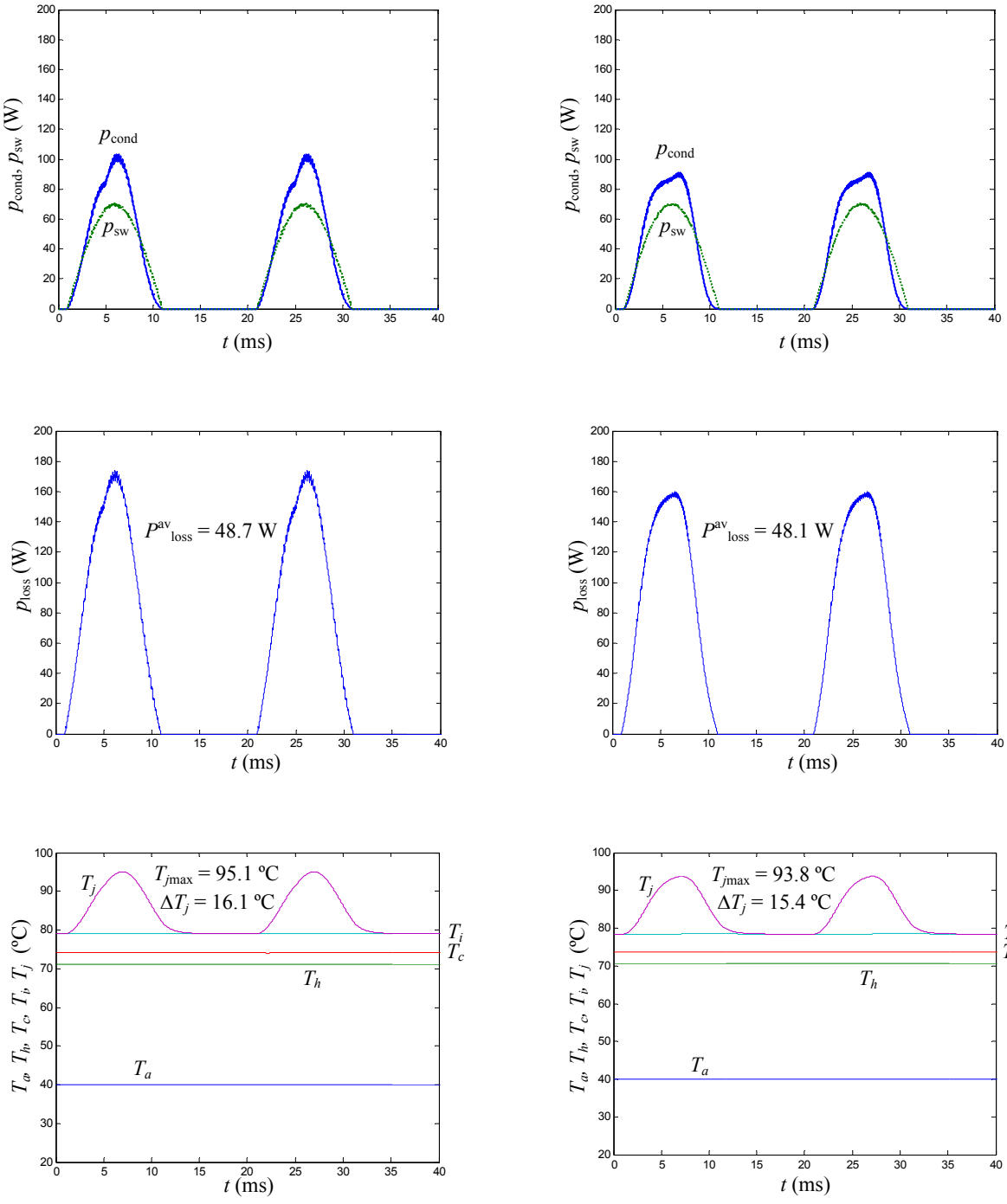
chapter produces a lower output-voltage distortion at around f_s ($V_{dis,1}$) and 2·f_s ($V_{dis,2}$). The maximum rms value of the harmonics around f_s ($V_{max,1}$) and 2·f_s ($V_{max,2}$) are also lower for the

ONTV^2 PWM. In general, both modulations are capable of controlling the neutral-point voltage in all three regions A, B, and C of Fig. 4.4, the ONTV^2 PWM presenting a lower output-voltage distortion. This benefit in output-voltage distortion is obtained for the same number of overall switching transitions. However, it should be noted that, in the ONTV^2 PWM, the duty-ratio pattern depends on the load power factor whereas it does not in the NTV^2 PWM.

From a losses/thermal point of view, the performance of the ONTV^2 PWM is similar to that of the NTV^2 PWM for high modulation indexes (worst case) since for these cases K_{opt} is almost zero, and the ONTV^2 PWM is therefore almost identical to the NTV^2 PWM. At other operating points the results of the comparison are not so clear. Figs. 4.6–4.10 show the simulation results, at m = 0.75 and a particular load, for the device's losses and converter temperatures, with the NTV^2 and ONTV^2 PWM. Table 4.2 presents a summary of these results. The differences are not quite significant. They are summarized as follows:

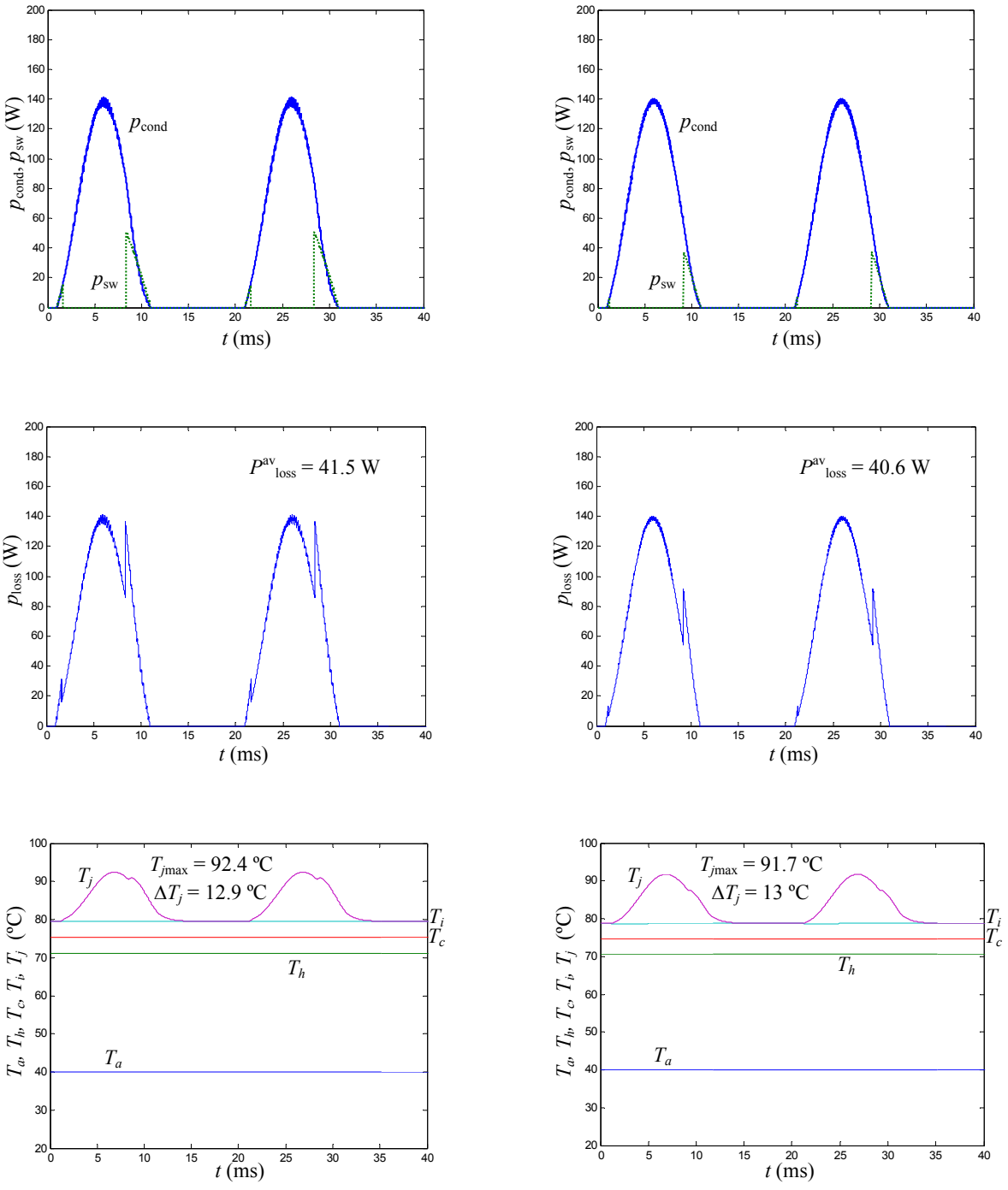
- In the ONTV^2 PWM, there is a transfer of conduction losses from the outer switches and outer and inner diodes to the inner switches and clamping diodes.
- The ONTV^2 PWM presents lower switching losses in the inner switches. This is due to a decrease in the number of commutations, thanks to a reduction of the line-cycle angle interval where both the phase duty-ratios of connection to p and n are different from zero.
- Overall, the ONTV^2 PWM has lower losses than the NTV^2 PWM and the heat sink temperature is slightly lower.
- All devices $T_{j\max}$ and ΔT_j are lower for the ONTV^2 PWM, except for the clamping diodes.

Fig. 4.11 presents the results obtained varying the inductive load angle. It can be seen that the ONTV^2 PWM presents a slightly better performance, especially at low load angles.



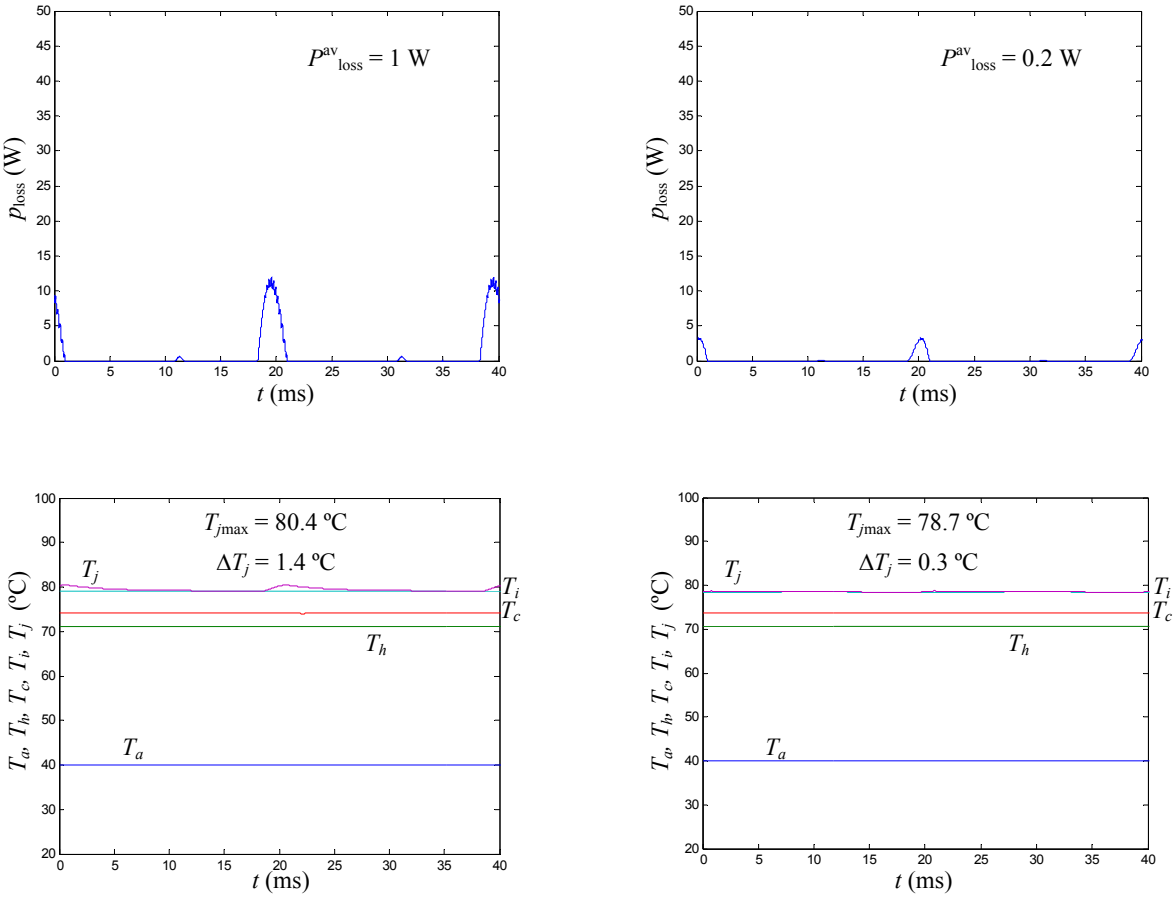
(a) *(b)*

Fig. 4.6. Outer switches (S_i, i = 1, 2…6). Conduction, switching, and total losses. Ambient, heat sink, and device temperatures. Conditions: T_a = 40 ºC, V_{pn} = 1500 V, m = 0.75, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 1 mF, R_L = 10 Ω, C_L = 0 F, and L_L = 10 mH (φ = 17.5º, Output Power = 54 kW).
(a) NTV² PWM. (b) ONTV² PWM.



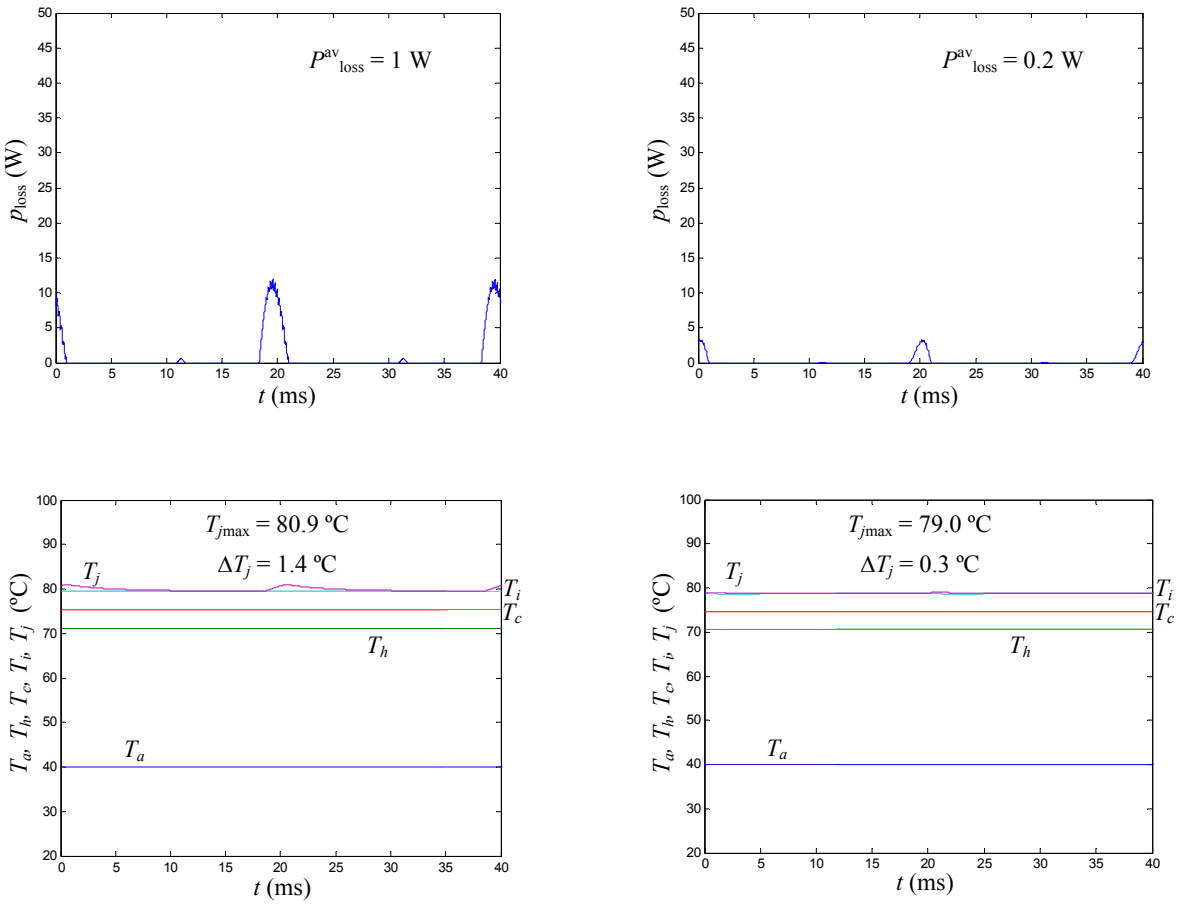
(a) *(b)*

Fig. 4.7. Inner switches (S_{ii}, i = 1, 2…6). Conduction, switching, and total losses. Ambient, heat sink, and device temperatures. Same conditions as in Fig. 4.6. (a) NTV² PWM. (b) ONTV² PWM.



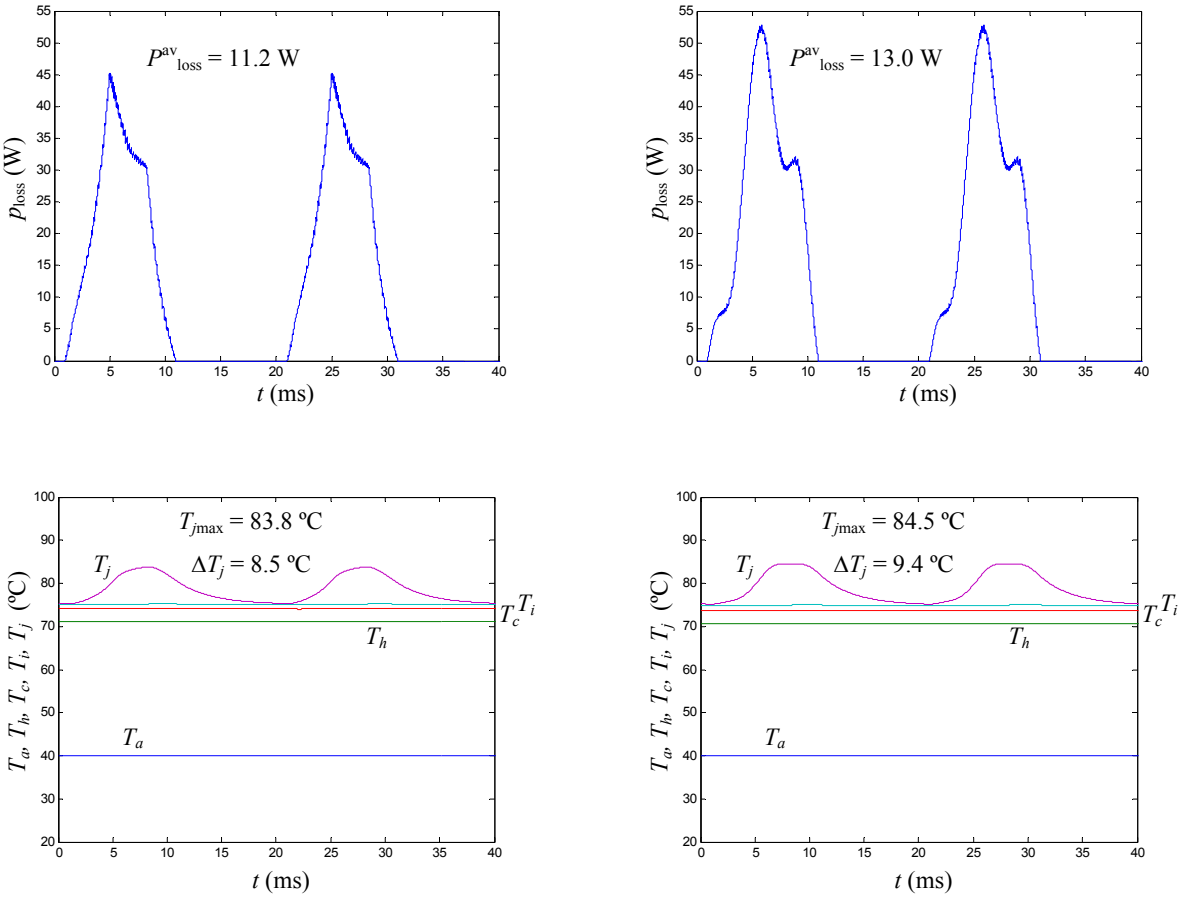
(a) *(b)*

Fig. 4.8. Outer diodes (D_i, i = 1, 2…6). Total losses. Ambient, heat sink, and device temperatures. Same conditions as in Fig. 4.6. (a) NTV² PWM. (b) ONTV² PWM.



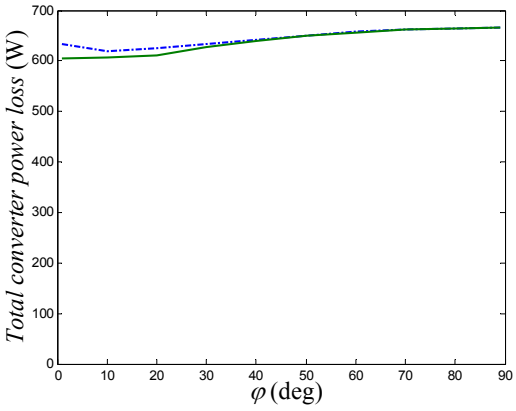
(a) *(b)*

Fig. 4.9. Inner diodes (D_{ii}, i = 1, 2…6). Total losses. Ambient, heat sink, and device temperatures. Same conditions as in Fig. 4.6. (a) NTV² PWM. (b) ONTV² PWM.

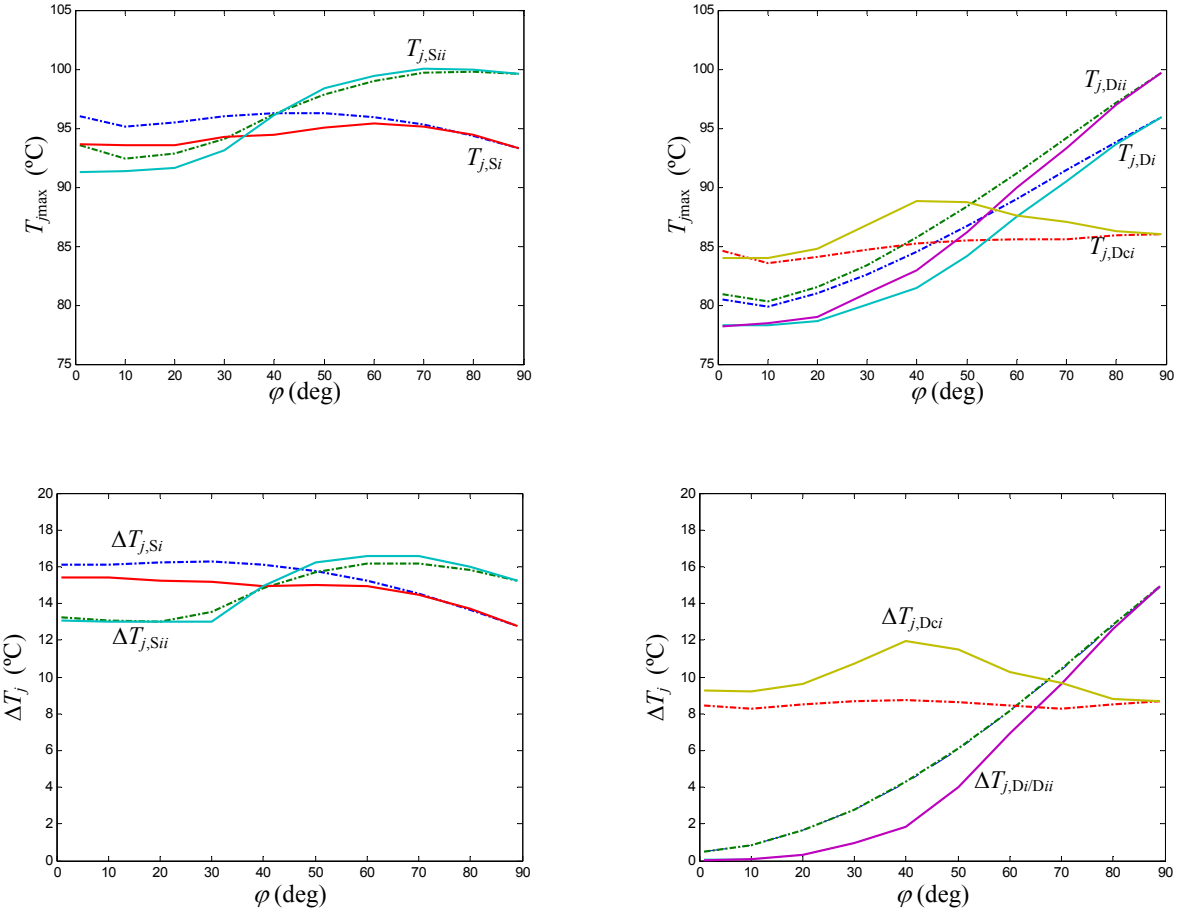


(a) *(b)*

Fig. 4.10. Clamping diodes (D_{ci}, i = 1, 2…6). Total losses. Ambient, heat sink, and device temperatures. Same conditions as in Fig. 4.6. (a) NTV² PWM. (b) ONTV² PWM.



(a)



(b) *(c)*

Fig. 4.11. Total converter power loss, maximum device junction temperature, and junction temperature variation as a function of the load angle. Conditions: Same conditions as in Fig. 4.6 and a fixed per-phase ac-load impedance Z_L = 10.48 Ω. (a) Total converter power loss. (b) Outer and inner switches. (c) Outer, inner, and clamping diodes. (Dash-dot: NTV² PWM. Solid: ONTV² PWM)

NTV² | ONTV²	***Module A***			***Module B***		***Converter Total***
	Outer Switch	**Outer Diode**	**Clamping Diode**	**Inner Switch**	**Inner Diode**	
P^{av}_{cond} (W)*	26.6 | 25.8	1.0 | 0.2	11.2 | 13.0	37.7 | 38.8	1.0 | 0.2	465.0 | 468.0
P^{av}_{sw} (W)	22.1 | 22.3	----	----	3.8 | 1.8	----	155.4 | 144.6
P^{av}_{loss} (W)	48.7 | 48.1	1.0 | 0.2	11.2 | 13.0	41.5 | 40.6	1.0 | 0.2	620.4 | 612.6
T_h (ºC)	71.0 | 70.6					
T_c (ºC)	74.1 | 73.7			75.2 | 74.7		
$T_{j\max}$ (ºC)	95.1 | 93.8	80.4 | 78.7	83.8 | 84.5	92.4 | 91.7	80.9 | 79.0	
ΔT_j (ºC)	16.1 | 15.4	1.4 | 0.3	8.5 | 9.4	12.9 | 13.0	1.4 | 0.3	

Table 4.2. Converter temp. and average losses for the NTV² and ONTV² PWM in the conditions of Fig. 4.6.

4.3.2. ONTV² vs. Song PWM

In Fig. 4.12, the proposed modulation is compared to the Song PWM, at a point in the m-φ operating plane where the Song PWM is able to achieve dc-link voltage balancing. It can also be seen that the distortion figures $V_{dis,1}$ and $V_{dis,2}$ for the ONTV² PWM are significantly lower.

In general, the Song PWM is only capable of controlling the neutral-point voltage in regions A and B (the same as for any other modulation that belongs to the NTV PWM family), with an output-voltage distortion at around f_s higher than in the case of the ONTV² PWM. However, these benefits in output-voltage distortion in regions A and B, and in the control of the neutral-point voltage in region C, are obtained at the expense of a higher number of overall switching transitions, for the same switching frequency. The ONTV² PWM requires 4/3 the number of commutations in the Song PWM.

Finally, it should be highlighted that the proposed modulation is able to almost completely suppressing the voltage distortion $V_{dis,1}$ for $m \leq 0.5$.

* Superscript 'av' indicates average value over a line cycle.

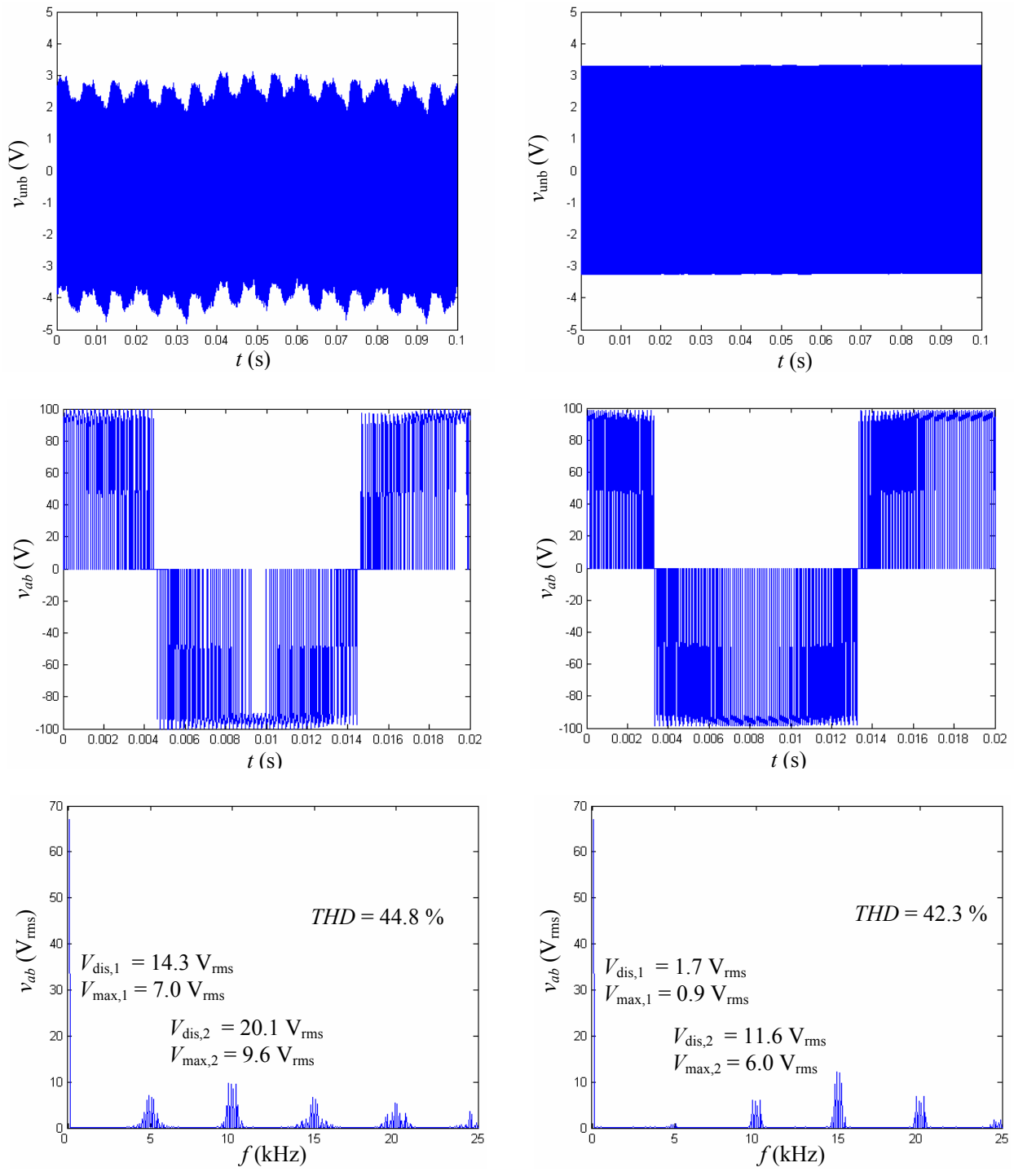


Fig. 4.12. Simulation results for v_{unb}, output voltage v_{ab}, and FFT(v_{ab}) *in the conditions: V_{pn} = 190 V, m = 0.5, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 100 μF, R_L = 2.72 Ω, C_L = 0 F, and L_L = 5 mH (φ = 30°). (a) Song PWM. (b) ONTV² PWM.*

4.4. Experimental Results

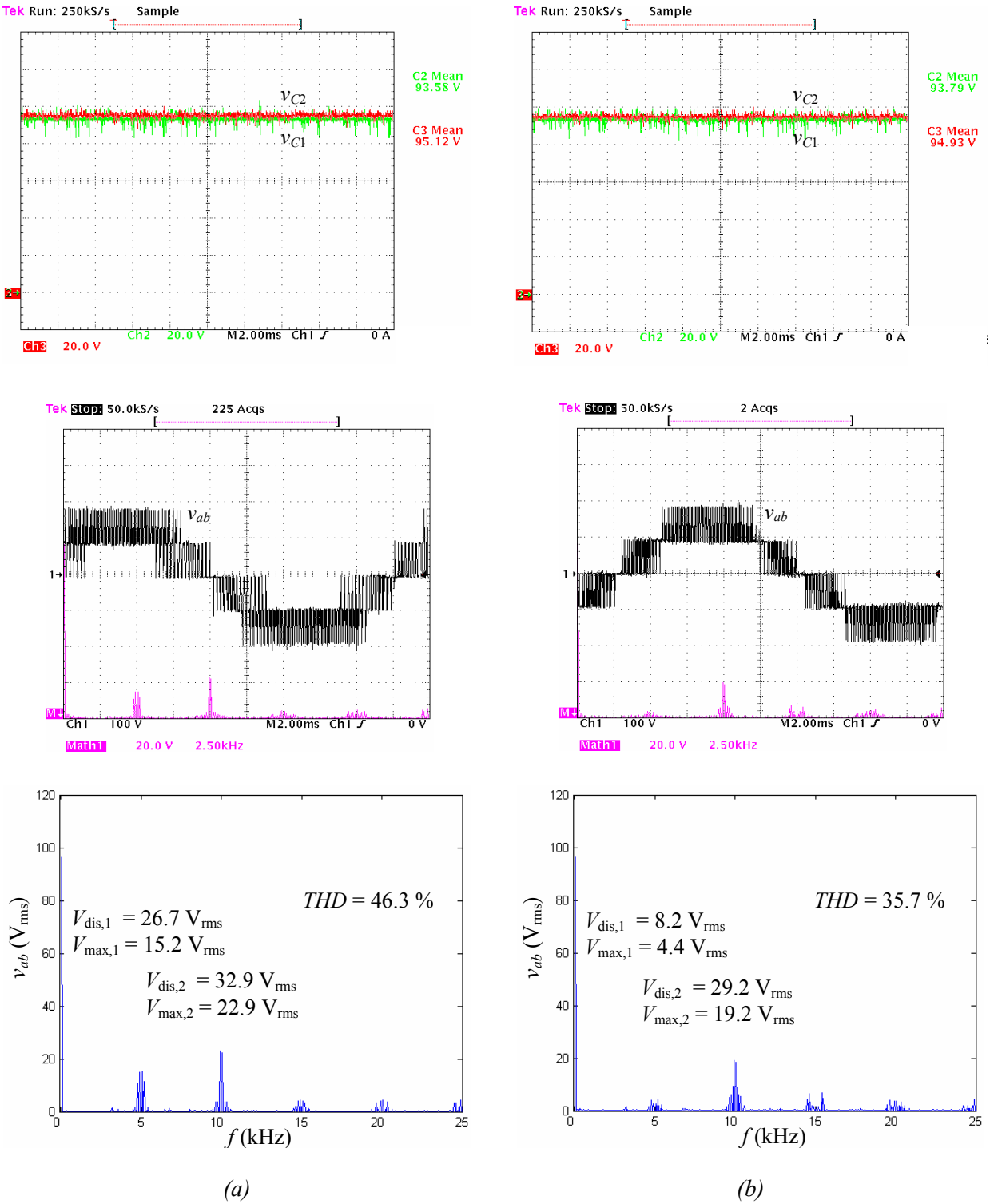
The performance of the proposed modulation has been experimentally verified in open loop using the prototype shown in Fig. 1.2(b), with the test setup described in Chapter 2 and detailed in Appendix A. In this case, the PowerPC in the dSPACE 1103 board computes d_{ap}, d_{bp}, d_{cp}, d_{an}, d_{bn}, d_{cn}, using (4.1) and (4.4)–(4.7).

Fig. 4.13 shows the experimental results obtained in the conditions of Fig. 4.5. It can be seen from both figures that there is good agreement between simulations and experiments.

Fig. 4.14 presents the results of the ONTV^2 PWM for an operating point in region C. The average i_o in each switching cycle is zero, guaranteeing the control of the neutral-point voltage. However, this is achieved with a $V_{\text{dis},1}$ value higher than for lower modulation indexes. Still, the distortion levels are lower than those for the NTV^2 PWM ($V_{\text{max},1}$ = 19.5 V_{rms}, $V_{\text{max},2}$ = 13.5 V_{rms}, from Chapter 2).

4.5. Conclusions

A new PWM for the comprehensive dc-link capacitor voltage balancing in the 3L-3P NPC VSI has been presented. The balancing of the neutral-point voltage is achieved over the full range of converter output voltages and for all load power factors with the minimum output-voltage switching-frequency distortion. Thus, for a given specification of maximum output-voltage distortion, the proposed modulation allows reducing the size of the dc-link capacitors and the output filter. Its benefits over other proposed modulation solutions have been verified through simulation and experiments. The proposed solution is also attractive due to the simple pattern of the phase duty-ratios in *d-q-0* coordinates.



(a) *(b)*

Fig. 4.13. Experimental results for v_{C1} and v_{C2} [20 V/div], output voltage v_{ab} [100 V/div], and FFT(v_{ab}) *in the conditions of Fig. 4.5. (a) NTV² PWM. (b) ONTV² PWM.*

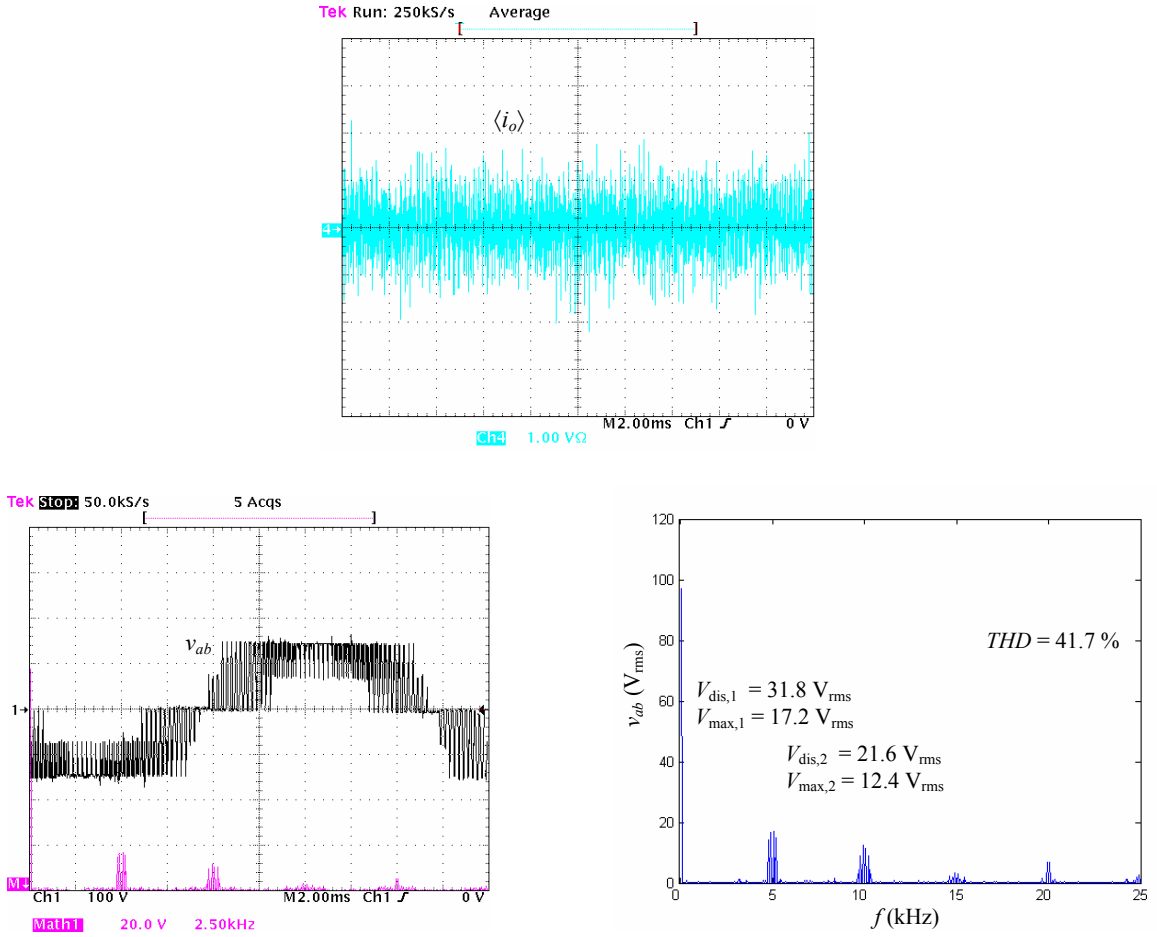


Fig. 4.14. Experimental results for $\langle i_o \rangle$ [1 A/div], output voltage v_{ab} [100 V/div], and FFT(v_{ab}) *for the ONTV² PWM in the following conditions: V_{pn} = 150 V, m = 0.95, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 1.1 mF, R_L = 11 Ω, C_L = 0 F, and L_L = 10 mH (φ = 15.94°).*

CHAPTER 5

CLOSED-LOOP CONTROL

Abstract — This chapter discusses the issues involved in the closed-loop design of the three-level three-phase neutral-point-clamped dc-ac converter using the optimized nearest-three virtual-space-vector pulsewidth modulation. The main part of the control is analogous to the control of a two-level converter, with an appropriate interfacing to the selected modulation, including an online estimation of the load angle at no extra cost. A specific loop is designed to control perturbations in the dc-link capacitor voltage balance. The closed-loop control is conceived and designed for a particular application and its performance is analyzed through simulation and experiments.

5.1. Introduction

In the previous chapter we have presented the ONTV^2 PWM, a generalization of the NTV^2 PWM that also allows comprehensively controlling the neutral-point voltage but with a lower output-voltage harmonic distortion in the case of linear and balanced loads. Once the modulation strategy has been defined, we just need to decide how we use the converter measures to determine the inputs to this modulation; i.e., only the converter closed-loop control remains to be designed.

This chapter discusses the issues involved in the closed-loop design of the 3L-3P NPC VSI using the ONTV^2 PWM. The closed-loop design is presented for a particular application and its performance is verified through simulation and experiments.

5.2. Review of the Optimized Nearest-Three Virtual-Space-Vector PWM

Let us remember that we designate as d_{ap}, d_{bp}, d_{cp}, d_{an}, d_{bn}, d_{cn} the six independent converter phase duty-ratios, where d_{xy} refers to the duty ratio of the phase x connection to the dc-link point y. Equation (5.1) reproduces from Chapter 4 the six expressions that define the ONTV^2 PWM in terms of these six independent phase duty-ratios in *d-q-0* coordinates (d_{pd}, d_{pq}, d_{p0}, d_{nd}, d_{nq}, d_{n0}).

$$\begin{aligned} d_{pd} &= \tan(\varphi)\cdot d_{pq} + m/\sqrt{2} \\ d_{nd} &= d_{pd} - \sqrt{2}\cdot m \\ d_{nq} &= d_{pq} \end{aligned} \tag{5.1}$$

$$\begin{cases} \theta \le 2\pi/3: \;\; d_{p0} = \sqrt{2}\cdot\left(-d_{pd}\cdot\cos(\theta+2\pi/3)+d_{pq}\cdot\sin(\theta+2\pi/3)\right) \\ 2\pi/3 < \;\theta \le 4\pi/3: \;\; d_{p0} = \sqrt{2}\cdot\left(-d_{pd}\cdot\cos(\theta)+d_{pq}\cdot\sin(\theta)\right) \\ \theta > 4\pi/3: \;\; d_{p0} = \sqrt{2}\cdot\left(-d_{pd}\cdot\cos(\theta-2\pi/3)+d_{pq}\cdot\sin(\theta-2\pi/3)\right) \end{cases}$$

$$\begin{cases} \theta \le \pi/3\,,\; \theta > 5\pi/3: \;\; d_{n0} = \sqrt{2}\cdot\left(-d_{nd}\cdot\cos(\theta)+d_{nq}\cdot\sin(\theta)\right) \\ \pi/3 < \theta \le \pi: \;\; d_{n0} = \sqrt{2}\cdot\left(-d_{nd}\cdot\cos(\theta-2\pi/3)+d_{nq}\cdot\sin(\theta-2\pi/3)\right) \\ \pi < \theta \le 5\pi/3: \;\; d_{n0} = \sqrt{2}\cdot\left(-d_{nd}\cdot\cos(\theta+2\pi/3)+d_{nq}\cdot\sin(\theta+2\pi/3)\right) \end{cases}$$

$$d_{pq} = -K\cdot\sin(3\theta)$$

where m is the modulation index ($m \in [0, 1]$) and θ is the angle of the reference vector $\mathbf{V}_{ref}$ with reference to α axis ($\mathbf{V}_{ref} = m\cdot e^{j\theta}$). The reference vector represents the desired fundamental converter three-phase voltage. The expressions in (5.1) assume that axis *d* of the *d-q-0* transformation of the phase duty-ratios is aligned with $\mathbf{V}_{ref}$.

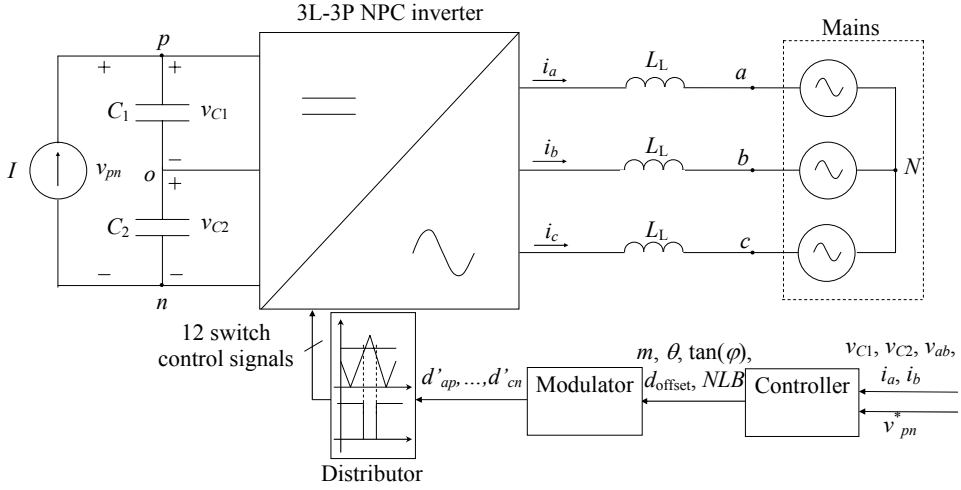
Variable φ is the load displacement angle and the optimum value of parameter K is a function of m and φ (4.10). In Chapter 4, expressions were provided to compute the value of K as a function of m and φ. Alternatively, a look-up table as a function of m and $\tan(\varphi)$ can be generated to select the appropriate value of K on-line.

Given the values of m, θ, and $\tan(\varphi)$, the duty ratios in *d-q-0* coordinates can be obtained from (5.1) and the look-up table or expressions (4.10) to compute K. Applying the inverse *d-q-0* transformation, we then obtain the independent phase duty-ratios d_{ap}, d_{bp}, d_{cp}, d_{an}, d_{bn}, d_{cn}. From these duty ratios and assuming that the sequence within a switching cycle of connection of each phase to each of the dc-link points is the symmetrical *p-o-n-o-p*, it is fairly straightforward to generate the twelve switch control signals.

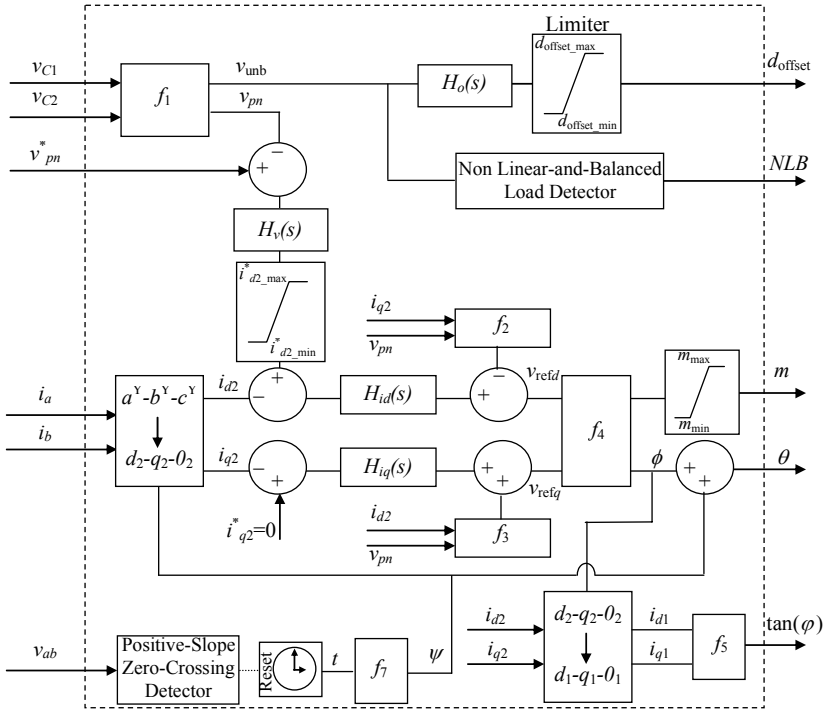
5.3. Closed-Loop Control Design

The proposed modulator and a controller have been designed and implemented for the particular system in Fig. 5.1(a). The purpose of the system is to send the energy generated by a dc current source to the mains with unity power factor while also regulating voltage v_{pn}. The control designed is applicable to any system where the power source connected to the inverter can be modeled as a dc current source and the energy is sent to the mains, such as, for example, a wind energy conversion system where the ac generator is connected to a non-controlled boost rectifier, and then to an inverter.

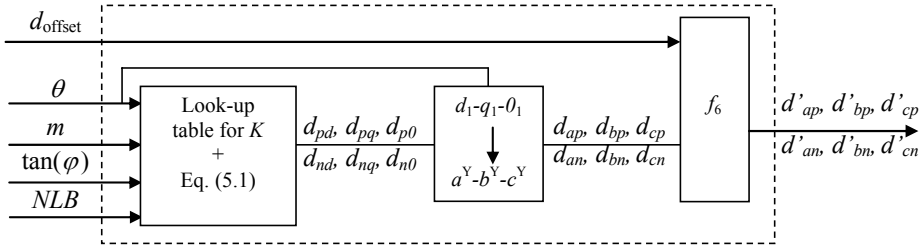
The diagrams of Fig. 5.1(b) and Fig. 5.1(c) summarize the controller and modulator structure, discussed in detail next.



(a)



(b)



(c)

Fig. 5.1. System block diagram. (a) Power stage plus control. (b) Controller. (c) Modulator.

5.3.1. Line-Cycle Average Neutral-Point Voltage Control

The ONTV^2 PWM guarantees no low-frequency oscillations of v_{unb} due to the loading conditions of the converter. Even if the load presents a severe non-linearity, this will not affect the dc-link voltage balance if we set $K = 0$ and the addition of line currents equals zero. However, the occurrence of neutral-point voltage perturbations due to other causes should be considered. Perturbations can occur if, for example, there is a leakage current flowing from the load neutral to ground (e.g., bearing currents [49]), causing that the addition of the three-phase currents be different from zero. The non-idealities, and specially the differences, in the switching behavior of the converter devices are another possible source of disturbances.

As discussed in [37], certain modulations for the 3L-3P NPC dc-ac converter have the property of naturally recovering the dc-link voltage balance after a perturbation. Hence, no special action is needed. The ONTV^2 PWM with $K = 0$ does not belong to this family of modulations. It does not affect the balance of the dc-link capacitors. If an unbalance exists at a given instant, the ONTV^2 PWM with $K = 0$ will preserve this unbalance (see Fig. 5.2(a)). However, the ONTV^2 with $K > 0$ does belong to the set of modulations that naturally recover the balance (see Fig. 5.2(b)). The higher the value of K, the faster the system recovers the balance (see Fig. 5.2(c)). Still, this natural recovery process is usually slow.

The addition of discharging resistors to the dc-link capacitors also helps recovering the balance after a perturbation. Their resistance value is usually high, though, and the recovery process thanks to these resistors is also slow (see Fig. 5.2(d)).

Since all preexisting possible balance recovery processes do not seem to be effective/fast enough, an appropriate perturbation of the modulating waveforms that allowed speeding-up this process would be helpful. Reference [26] shows that introducing a common-mode voltage into the line-to-neutral output-voltage waveforms causes an unbalance in the discharging of the dc-link capacitors. This is done by adding an offset (d_{offset}) to the d_{ap}–d_{an}, d_{bp}–d_{bn}, d_{cp}–d_{cn} modulating waveforms. This property can be used to speed-up the recovery process whenever a dc-link voltage unbalance occurs. Here, this control mechanism is adapted to the ONTV^2 PWM.

If we want to add an offset to the d_{ap}–d_{an} waveform, we have three options:

1) We add the offset to d_{ap}.

2) We subtract the offset from d_{an}.

3) We add part of the offset to d_{ap} and we subtract the remaining part from d_{an}.

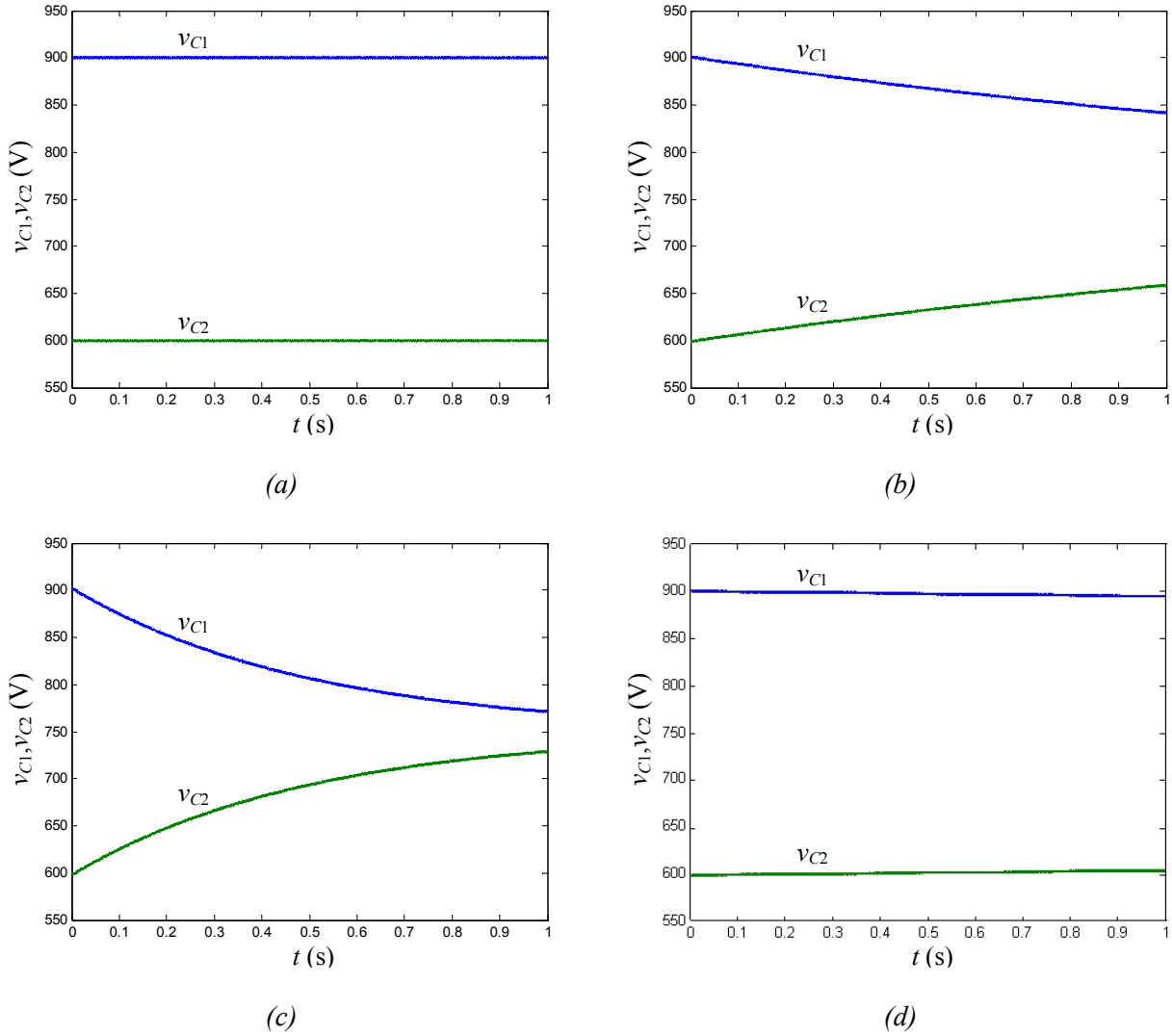


Fig. 5.2. Dc-link capacitor voltage balance recovery transient under the following conditions: V_{pn} = 1500 V, m = 0.75, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 1 mF, R_L = 10 Ω, and L_L = 10 mH. (a) ONTV^2 PWM, K = 0. (b) ONTV^2 PWM, K = 0.09. (c) ONTV^2 PWM, K = 0.18. (d) ONTV^2 PWM, K = 0, and 54 kΩ discharging resistors in parallel with each dc-link capacitor.

A simple and interesting strategy is to apply all the offset to the duty ratio to be reduced. Since duty ratios must be higher than zero, in case we reach the value of zero, the other duty ratio will be increased an amount corresponding to the part of the offset still not applied. This strategy allows minimizing the number of commutations, since it may cause a non-zero duty-ratio become zero. With reference to Fig. 5.1(c), this strategy can be formulated for phase x as

$d'_{ap} = f_{61}(d_{ap}, d_{an}, d_{\text{offset}})$; $d'_{bp} = f_{63}(d_{bp}, d_{bn}, d_{\text{offset}})$; $d'_{cp} = f_{65}(d_{cp}, d_{cn}, d_{\text{offset}})$;

$d'_{an} = f_{62}(d_{ap}, d_{an}, d_{\text{offset}})$; $d'_{bn} = f_{64}(d_{bp}, d_{bn}, d_{\text{offset}})$; $d'_{cn} = f_{66}(d_{cp}, d_{cn}, d_{\text{offset}})$;

```
if (d_offset ≥ 0) {
   if (d_xn > d_offset) {
      d'_xn = d_xn – d_offset
      d'_xp = d_xp
   }else {
      d'_xn = 0
      d'_xp = d_xp + (d_offset – d_xn)
   }
}else {
   if (d_xp > |d_offset|) {
      d'_xp = d_xp – |d_offset|
      d'_xn = d_xn
   }else {
      d'_xp = 0
      d'_xn = d_xn + (|d_offset| – d_xp)
   }
}
```

(5.2)

The value of d_{offset} to be applied is determined from the dc-link capacitor voltage unbalance $v_{\text{unb}} = f_{11}(v_{C1}, v_{C2}) = (v_{C2} - v_{C1}) / 2$ by a compensator. This compensator has a low-pass characteristic, in order to only react to line-cycle average perturbations of the dc-link voltage balance. It would be possible to use this type of control to correct any dc-link voltage unbalance (at any frequency). Any conventional NTV modulation, unable of controlling the neutral-point voltage, could be used in this case, and the neutral-point voltage would be free from any unbalance thanks to the offset introduced to the modulating duty-ratio waveforms. However, this solution would have a couple of drawbacks. First of all, significant common mode noise would be introduced. Second, the maximum modulation index would be limited. Using a modulation that inherently controls the low-frequency oscillations of v_{unb} is a more efficient solution, since the offset control must then only be in charge of correcting the sporadic perturbations that may occur in the dc-link voltage balance. Due to the minor action that this control does, the common-mode noise introduced is negligible and the modulation index can reach the maximum theoretical value of 1.

5.3.2. Non Linear-and-Balanced Load Detector

If the load is not quite linear and balanced, the ONTV^2 PWM will set $K = 0$ in order to maintain the neutral-point voltage control. This situation can be detected indirectly through sensing v_{unb}, detecting its peak value, and if it goes beyond a given maximum, activating and latching a non linear-and-balanced load flag (*NLB*) in order to force $K = 0$ in the modulator.

Other means of detecting the non linear-and-balanced load case could be to monitor the maximum length of the line-current vector oscillation in *d-q* coordinates.

5.3.3. Reference Vector Computation

From a closed-loop control point of view, the key difference between a two-level and a three-level dc-ac converter is that the latter introduces the dynamics of the neutral-point voltage.

We can assume that the neutral-point voltage is always balanced thanks to the chosen modulation and the dedicated control presented in the preceding section. Then, the average model of the 3L-3P NPC converter becomes equivalent to the model of a two-level converter. Hence, conventional control schemes and design procedures for the two-level converter can be directly applied to the three-level converter to obtain, from the sensed variables, the reference vector length m and angle θ required by the modulator.

For the particular application considered here, the selected control scheme is shown in Fig. 5.1(b). First, the dc-link voltage $v_{pn} = f_{12}(v_{C1}, v_{C2}) = v_{C1} + v_{C2}$ is compared to the desired command. The error is then processed by a compensator to produce the i_d command. Line currents i_a and i_b are sensed and *d-q* transformed. We do not need to sense i_c since we know $i_c = -i_a - i_b$. The transformation is performed to axes d_2-q_2-0_2, where axis d_2 is in phase with the vector of line-to-neutral mains voltages ($\mathbf{V}_{L\text{-}N}$). This vector has an angle ψ with reference to axis α (Fig. 5.3):

$$\psi = f_7(t) = \omega_o \cdot t - 2\pi/3. \tag{5.3}$$

The d_2 and q_2 components of the current are compared to their corresponding command. The i_{q2} command is zero to achieve a unity displacement factor for the power transferred to the mains. Both *d* and *q* channel errors are processed by their specific compensators. Finally, both channels are decoupled through f_2 and f_3:

$$\begin{aligned} f_2(i_{q2}, v_{pn}) &= \frac{\sqrt{2} \cdot i_{q2} \cdot \omega_o \cdot L_L}{v_{pn}} \\ f_3(i_{d2}, v_{pn}) &= \frac{\sqrt{2} \cdot i_{d2} \cdot \omega_o \cdot L_L}{v_{pn}}. \end{aligned} \tag{5.4}$$

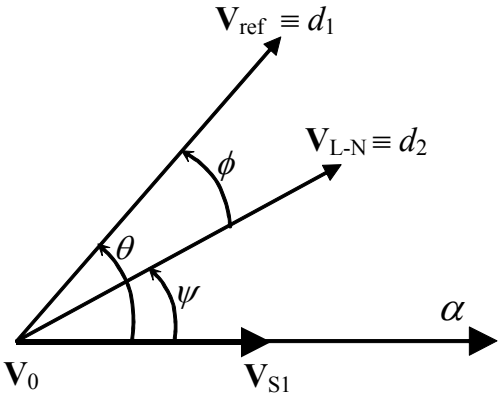


Fig. 5.3. Location of vectors $\mathbf{V}_{\text{ref}}$ *and* $\mathbf{V}_{\text{L-N}}$ *with reference to axis* α.

The outcome of both channels is the d_2 and q_2 components of $\mathbf{V}_{\text{ref}}$. Through f_4 we obtain the $\mathbf{V}_{\text{ref}}$ length m (modulation index) and angle ϕ (with respect to axis d_2):

$$\begin{aligned} m &= f_{41}\left(v_{\text{ref}d}, v_{\text{ref}q}\right) = \sqrt{v_{\text{ref}d}^2 + v_{\text{ref}q}^2} \\ \phi &= f_{42}\left(v_{\text{ref}d}, v_{\text{ref}q}\right) = \tan^{-1}\left(\frac{v_{\text{ref}q}}{v_{\text{ref}d}}\right). \end{aligned} \tag{5.5}$$

Angle θ can then be obtained by simply adding ψ and ϕ (Fig. 5.3). This is the angle that will be used to perform the transformation of the duty ratios from d_1-q_1-0_1 to a^{Y}-b^{Y}-c^{Y} coordinates within the modulator.

5.3.4. Online Estimation of Tan(φ)

To implement the ONTV^2 PWM we need an estimate of tan(φ). Angle φ corresponds to the angle between the vector of fundamental line currents and $\mathbf{V}_{\mathbf{ref}}$. Hence, the value of tan(φ) can be computed online by simply sensing the line currents, applying the d_1-q_1 transformation, and using (5.6) (in the case of non linear-and-balanced loads, the dc values of the d_1 and q_1 components can be used.) Since, in general, the controller already requires sensing the line currents, the implementation of the ONTV^2 PWM does not require additional sensors.

$$\tan(\varphi) = f_5\left(i_{d1}, i_{q1}\right) = -\frac{i_{q1}}{i_{d1}}. \tag{5.6}$$

5.4. Simulation Results

Switching and average models of the closed-loop system have been implemented in Simulink. Simulation results are presented in the following sections.

5.4.1. Line-Cycle Average Neutral-Point Voltage Control

The line-cycle average neutral-point voltage control has been tested stand alone in the conditions of Fig. 5.2(a). The compensator transfer function and d_{offset} limits are

$$\begin{aligned} H_o(s) &= -0.2 \cdot \frac{(s + 2\pi \cdot 0.01)}{s \cdot (s + 2\pi \cdot 25)} \\ [d_{\text{offset\_min}}, \quad d_{\text{offset\_max}}] &= [-0.1, \quad 0.1]. \end{aligned} \tag{5.7}$$

The results in Fig. 5.4 show that this control allows quickly suppressing the dc-link voltage balance perturbations (much faster than the natural mechanisms) with little control effort. Note that after the balance is achieved $d_{\text{offset}} = 0$.

5.4.2. Complete Control

The remaining part of the control has been designed for the conditions of Fig. 5.5. The compensator transfer functions and variable limits are

$$\begin{aligned} H_o(s) &= -2 \cdot \frac{(s + 2\pi \cdot 0.01)}{s \cdot (s + 2\pi \cdot 25)} \\ H_v(s) &= -4000 \cdot \frac{(s + 2\pi \cdot 20)}{s \cdot (s + 2\pi \cdot 2500)} \\ H_{id}(s) &= 500 \cdot \frac{(s + 2\pi \cdot 80)}{s \cdot (s + 2\pi \cdot 2500)} \\ H_{iq}(s) &= 500 \cdot \frac{(s + 2\pi \cdot 3)}{s \cdot (s + 2\pi \cdot 2500)} \end{aligned} \tag{5.8}$$

$$\begin{aligned} [d_{\text{offset\_min}}, \quad d_{\text{offset\_max}}] &= [-0.1, \quad 0.1] \\ [i^*_{d2\_\text{min}}, \quad i^*_{d2\_\text{max}}] &= [-50, \quad 50] \\ [m_{\text{min}}, \quad m_{\text{max}}] &= [0, \quad 1]. \end{aligned}$$

Fig. 5.5 shows the results obtained with the complete closed-loop switching model for a step in voltage command v^*_{pn} from 800 V to 750 V. We can observe that there is no unbalance of the dc-link capacitor voltages before, during, and after the step transient, as expected. Since the ONTV^2 PWM already guarantees this balancing, the effort of the dedicated control is minimal (see Fig.

5.5(d)). In Fig. 5.5(f) we can observe that the power conversion is achieved with unity displacement factor, as intended.

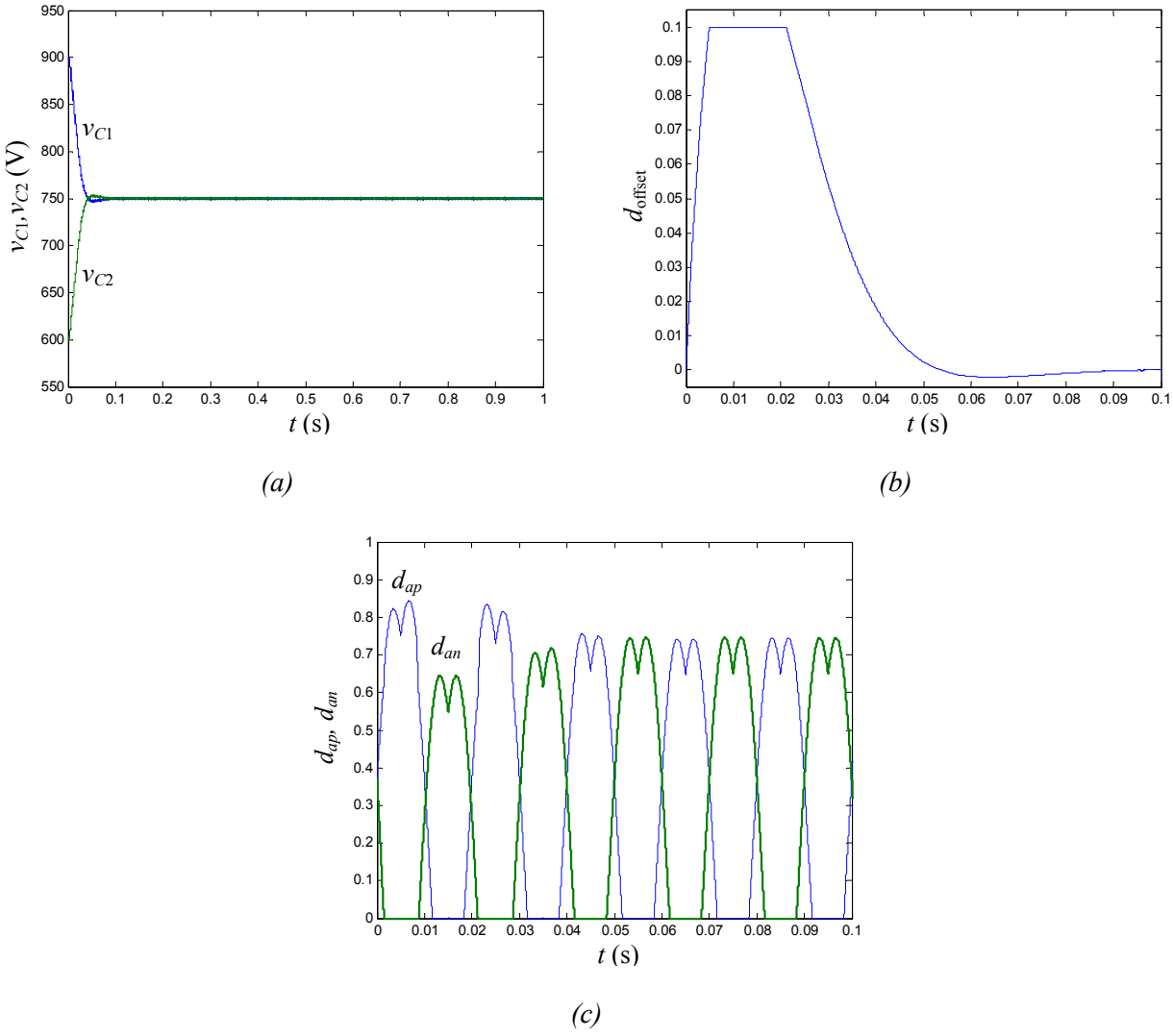


Fig. 5.4. Closed-loop dc-link voltage balance recovery transient under the conditions of Fig. 5.2(a). (a) v_{C1} and v_{C2}. (b) d_{offset}. (c) d_{ap} and d_{an}.

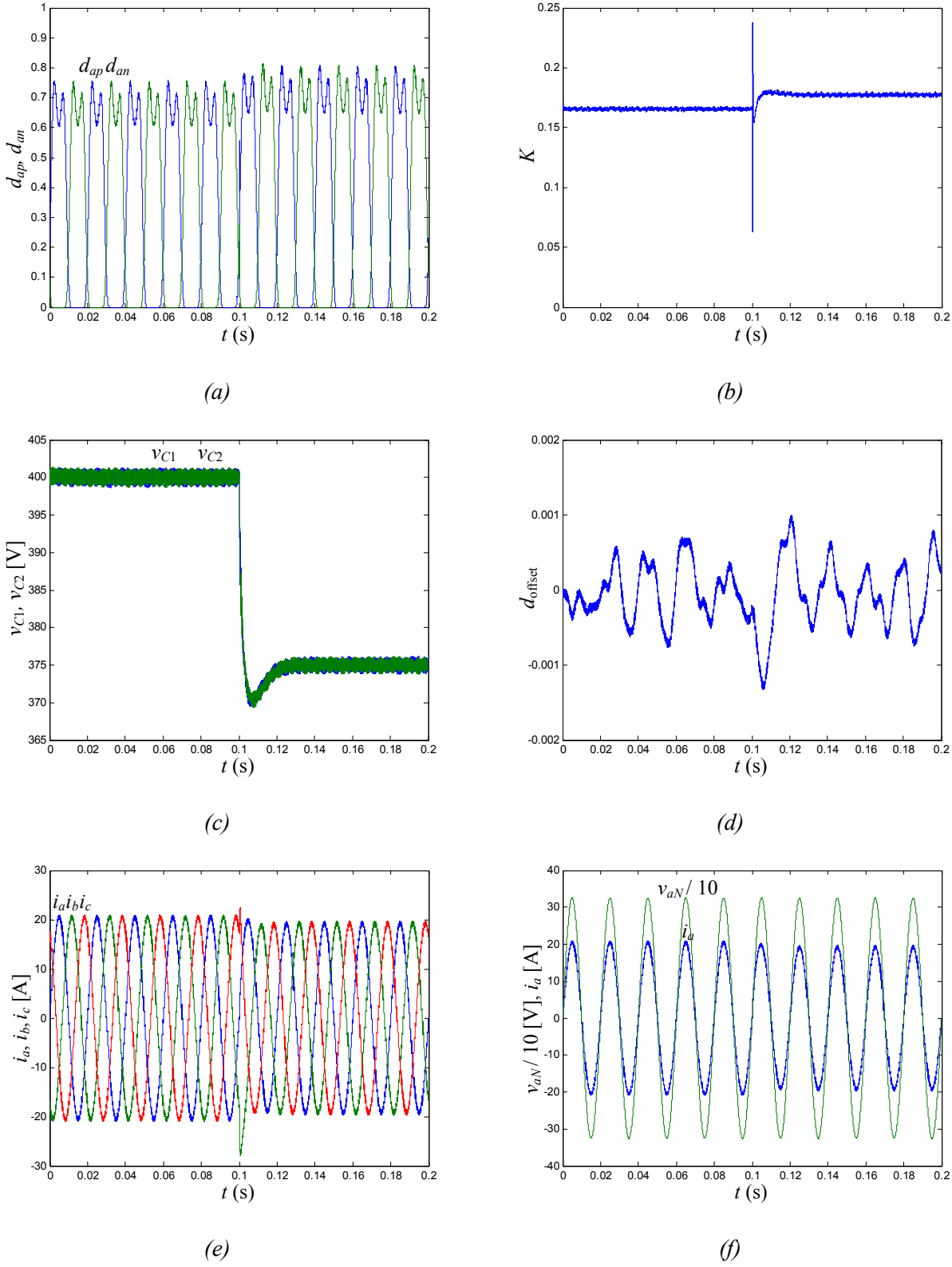


Fig. 5.5. Simulation results for a step in command v^*_{pn} at time = 0.1 s in the following conditions: I = 12.5 A, C_{dc} = 400 μF, L_L = 5mH, $V_{aN} = V_{bN} = V_{cN}$ =230 V_{rms}, f_o = 50 Hz, and f_s = 5 kHz. (a) d_{ap} and d_{an}. (b) Modulation parameter K. (c) Dc-link voltages v_{C1} and v_{C2}. (d) d_{offset}. (e) Three-phase currents i_a, i_b and i_c. (f) Mains voltage v_{aN} and line current i_a.

5.5. Experimental Results

Experimental tests have been conducted to further verify the correct performance of the proposed closed-loop control. The experiments have been carried out using the same prototype described in previous chapters.

5.5.1. Line-Cycle Average Neutral-Point Voltage Control

The performance of the dedicated control can be observed in Fig. 5.6. Fig. 5.6(a) shows the dc-link voltages without activating the control. There is a negligible dc unbalance possibly due to the different capacitance of the dc-link capacitors. This small dc unbalance is corrected when the control is activated (Fig. 5.6(b)). The balancing is achieved with little control effort.

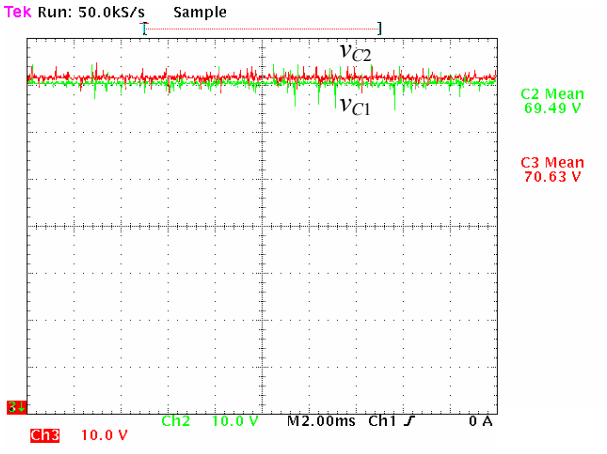
The control is capable of correcting any other higher dc unbalance or of achieving any desired operating dc-link voltages, as demonstrated in Fig. 5.6(c), where the control is tuned to achieve a $v_{\text{unb}} = -5$ V. As expected, the control effort to achieve this operating point is higher than in the previous case.

5.5.2. Complete Control

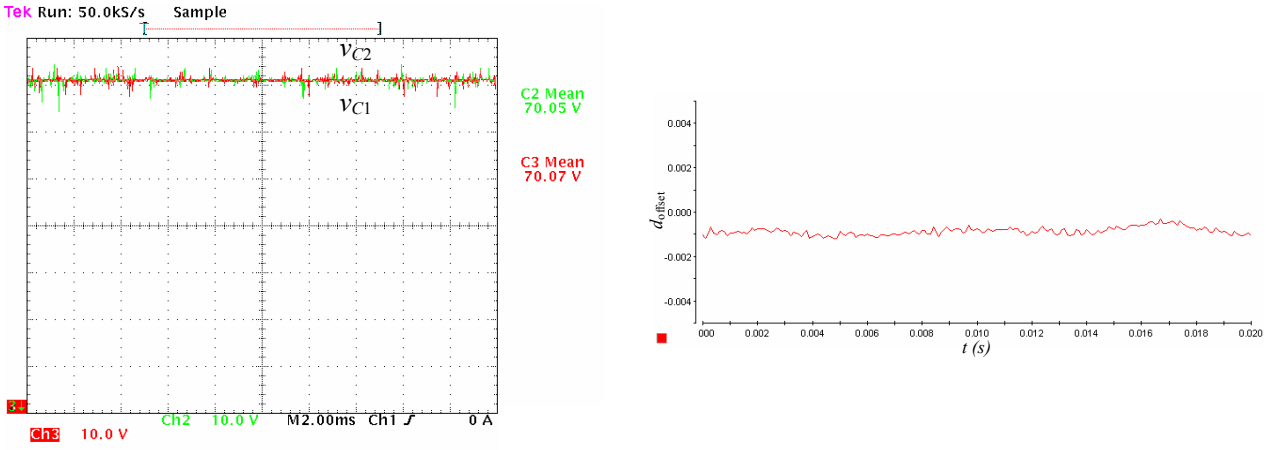
Fig. 5.7 shows the experimental results obtained with the complete control for a step in voltage command v^*_{pn} from 150 V to 130 V. A dc power supply acts as the dc current source. A transformer-autotransformer set has been used to provide isolation and to step down the mains voltage. The controller used is

$$
\begin{aligned}
H_o(s) &= -2 \cdot \frac{(s + 2\pi \cdot 0.01)}{s \cdot (s + 2\pi \cdot 25)} \\
H_v(s) &= -5000 \cdot \frac{(s + 2\pi \cdot 1.5)}{s \cdot (s + 2\pi \cdot 2500)} \\
H_{id}(s) &= 500 \cdot \frac{(s + 2\pi \cdot 15)}{s \cdot (s + 2\pi \cdot 2500)} \\
H_{iq}(s) &= 1000 \cdot \frac{(s + 2\pi \cdot 5)}{s \cdot (s + 2\pi \cdot 2500)}
\end{aligned}
\tag{5.9}
$$

$$
\begin{aligned}
\left[d_{\text{offset\_min}},\ \ d_{\text{offset\_max}}\right] &= \left[-0.1,\ \ 0.1\right] \\
\left[i^*_{d2\_\text{min}},\ \ i^*_{d2\_\text{max}}\right] &= \left[-10,\ \ 10\right] \\
\left[m_{\text{min}},\ \ m_{\text{max}}\right] &= \left[0,\ \ 1\right].
\end{aligned}
$$



(a)



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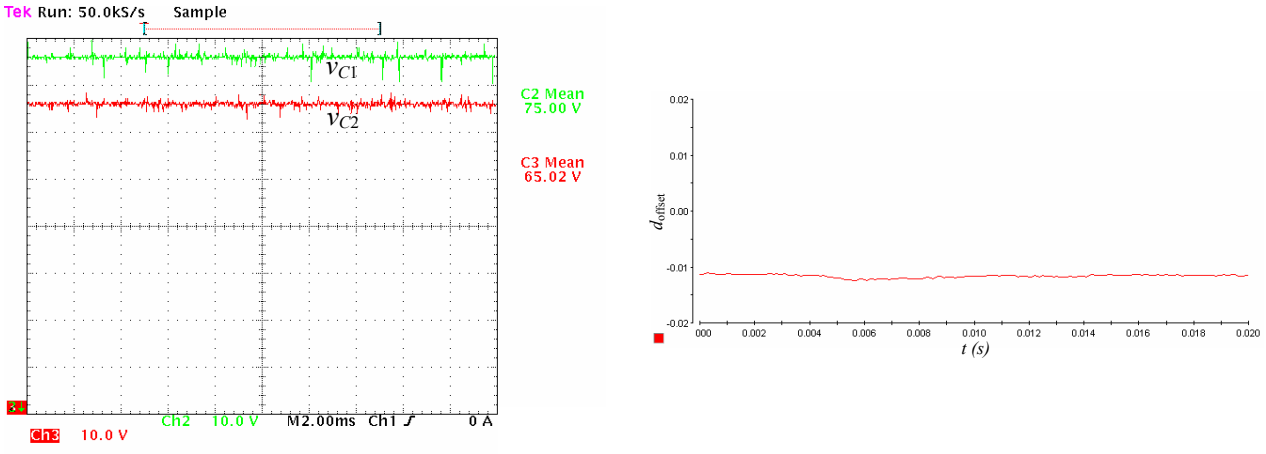
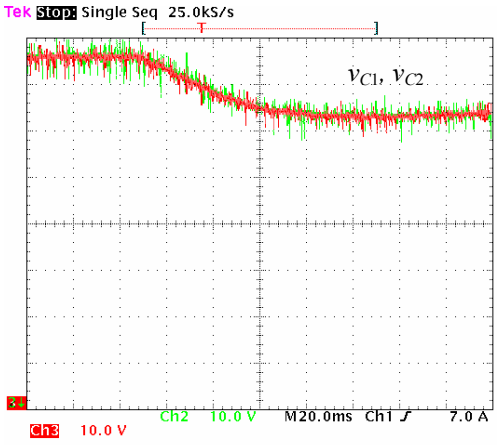
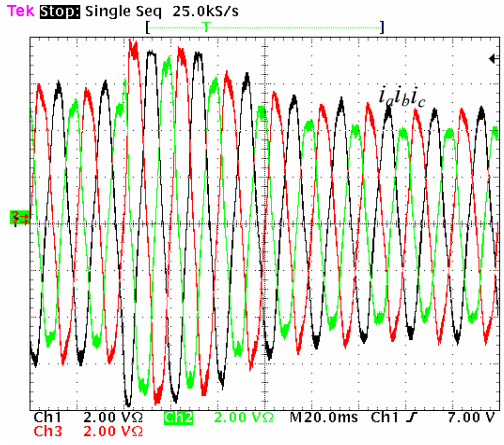


(c)

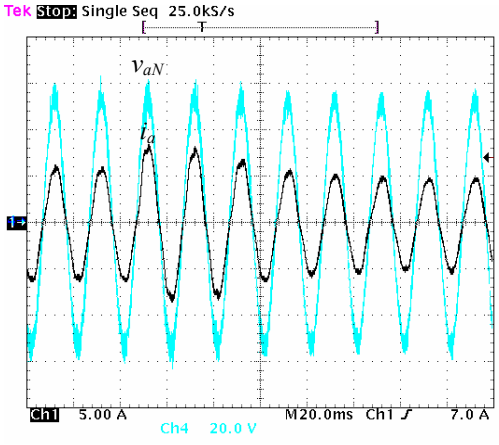
Fig. 5.6. Line-cycle average neutral-point voltage control performance in the following conditions: NTV² PWM, V_{pn} = 140 V, m = 0.75, f_o = 50 Hz, f_s = 5 kHz, C_{dc} = 1.1 mF, R_L = 16.5 Ω, and L_L = 5 mH. (a) Dedicated control off. (b) Dedicated control on. (c) Dedicated control on, tuned to achieve v_{unb} = –5 V.



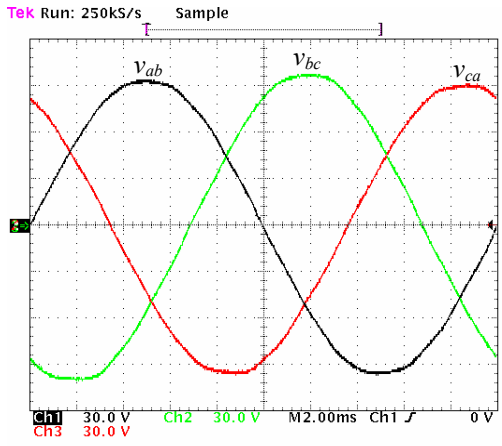
(a)



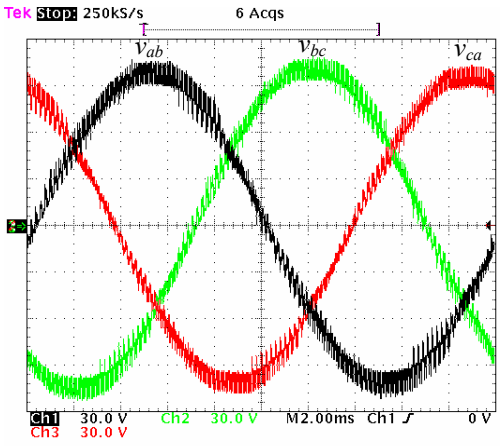
(b)



(c)



(d)



(e)

Fig. 5.7. Experimental results for a step in command v^*_{pn} in the following conditions: I = 4 A, C_{dc} = 1.1 mF, L_L = 10 mH, $V_{aN} = V_{bN} = V_{cN}$ = 40 V_{rms}, f_o = 50 Hz, and f_s = 5 kHz. (a) v_{C1} and v_{C2} [10 V/div]. (b) Three-phase currents i_a, i_b and i_c [2 A/div]. (c) Mains voltage v_{aN} [20 V/div] and line current i_a [5 A/div]. (d) Mains voltages v_{ab}, v_{bc}, and v_{ca} [30 V/div] (converter off). (e) Mains voltages v_{ab}, v_{bc}, and v_{ca} (converter on).

The transient takes longer than expected (with an ideal current source) due to a 2 mF capacitance at the output of the dc power supply. The asymmetry of the ac voltage applied (Fig. 5.7(d)) causes the differences in the peak line-current levels among the three phases. Note also the significant line inductance introduced by the transformer-autotransformer set (Fig. 5.7 (e)).

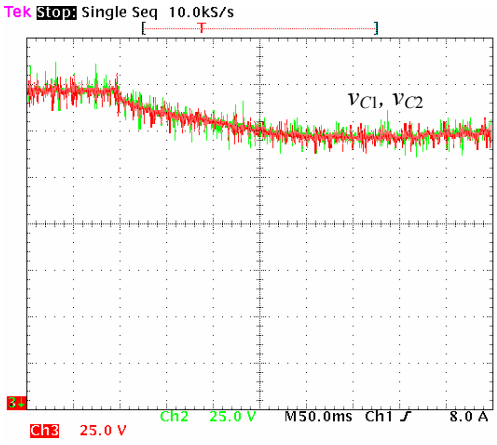
Fig. 5.8 shows the experimental results obtained connecting a rectified wind mill generator voltage to the dc-link, according to Fig. 2.17. A constant torque of 10 Nm is applied to the generator shaft to emulate the wind torque. A step in v^*_{pn} from 340 V to 300 V is forced, producing a variation of the rotor speed from 1577 rpm to 1396 rpm. The controller employed in this case is

$$\begin{aligned} H_o(s) &= -2 \cdot \frac{(s + 2\pi \cdot 0.01)}{s \cdot (s + 2\pi \cdot 25)} \\ H_v(s) &= -1000 \cdot \frac{(s + 2\pi \cdot 5)}{s \cdot (s + 2\pi \cdot 2500)} \\ H_{id}(s) &= 500 \cdot \frac{(s + 2\pi \cdot 25)}{s \cdot (s + 2\pi \cdot 2500)} \\ H_{iq}(s) &= 1000 \cdot \frac{(s + 2\pi \cdot 5)}{s \cdot (s + 2\pi \cdot 2500)} \end{aligned} \tag{5.10}$$

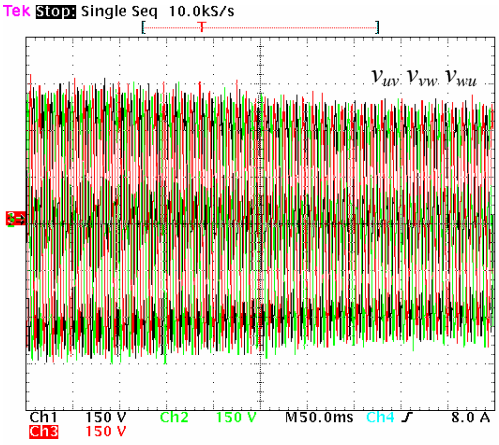
$$\begin{aligned} [d_{\text{offset\_min}}, \quad d_{\text{offset\_max}}] &= [-0.1, \quad 0.1] \\ [i^*_{d2\_\text{min}}, \quad i^*_{d2\_\text{max}}] &= [-10, \quad 10] \\ [m_{\text{min}}, \quad m_{\text{max}}] &= [0, \quad 1]. \end{aligned}$$

5.6. Conclusions

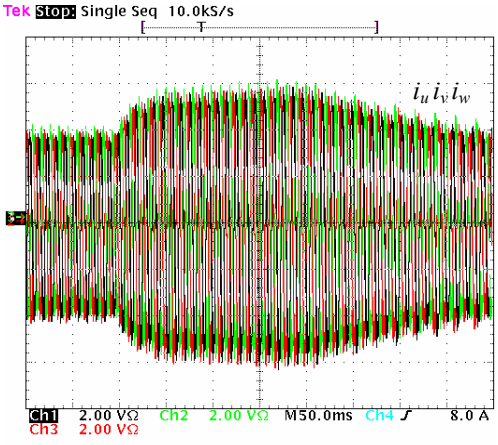
A closed-loop design of the 3L-3P NPC dc-ac converter using the ONTV^2 PWM has been presented. The selected modulation allows using small dc-link capacitors leading to an improved performance of the closed-loop system. The control structure is analogous to the one used for a two-level converter, with an appropriate interfacing to the modulation (including an online estimation of the load angle at no extra cost), and the addition of a dedicated loop to deal with line-cycle average perturbations in the dc-link capacitor voltage balance. The proper performance of the control has been verified through simulation and experiments.



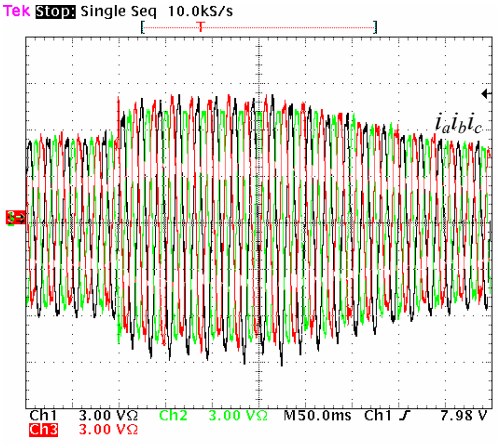
(a)



(b)



(c)



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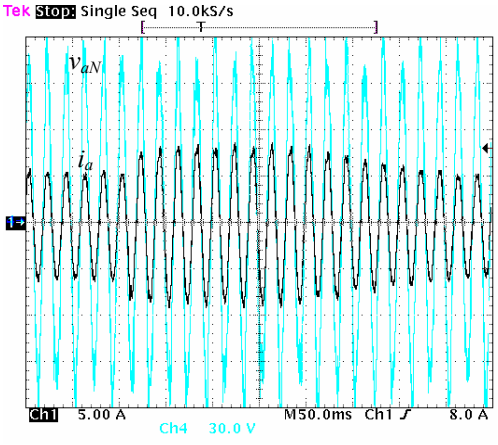


(e)

Fig. 5.8. Experimental results for a step in command v^*_{pn}. Conditions: Rectified wind mill generator voltage, L_S = 12.5 mH, C_{dc} = 1.1 mF, L_L = 10 mH, $V_{aN} = V_{bN} = V_{cN}$ = 75 V_{rms}, f_o = 50 Hz, and f_s = 5 kHz. (a) Dc-link voltages v_{C1} and v_{C2} [25 V/div]. (b) Generator voltages v_{uv}, v_{vw}, and v_{wu} [150 V/div]. (c) Generator currents i_u, i_v, and i_w [2 A/div]. (d) i_a, i_b and i_c [3 A/div]. (e) Mains voltage v_{aN} [30 V/div] and line current i_a [5 A/div].

CHAPTER 6

CONCLUSIONS

Abstract — This chapter summarizes the thesis contributions and discusses the possible future extensions of the research accomplished.

6.1. Contributions

The main contribution of the present thesis is the definition of the ONTV^2 PWM. The ONTV^2 PWM is applicable to the 3L-3P NPC dc-ac converter with any system connected at the dc and ac sides, provided that the addition of the ac-side line currents equals zero. This modulation allows controlling the neutral-point voltage under any operating condition with a low output-voltage switching-frequency distortion. The modulation pattern is the same for any non-linear or unbalanced ac-side load/source. Under linear-and-balanced ac-side loads/sources, the modulation pattern varies with the load/source angle, as seen from the converter ac side. In any case, though, the modulation pattern is fairly simple and has been mathematically characterized as a function of the modulation index, line-cycle angle, and load angle (linear-and-balanced loads). The modulation computational cost is comparable to the cost of any other conventional PWM. For the same switching frequency, the proposed PWM produces a higher number of switching transitions compared to other conventional PWM. However, the resulting increase in thermal stress is typically negligible. The suppression of low-frequency oscillations in the neutral-point voltage may allow a significant reduction of the dc-link capacitance leading to a reduction in the converter cost, size and weight, and also to an improvement in the system reliability and dynamical performance.

Other contributions can be summarized as follows:

- The particular and simple modulation pattern of the ONTV^2 PWM corresponding to non linear-and-balanced ac-side loads/sources can also be used for any type of ac-side load/source, defining what we designate as the NTV^2 PWM. This modulation has the advantage of being independent of the ac load/source angle, allowing for a more robust implementation of the neutral-point control since it is not dependent upon the ac load/source angle measurement/estimation accuracy. The drawback is an increased output-voltage high-frequency distortion under linear-and-balanced ac-side loads/sources compared to the ONTV^2 PWM.

- A necessary step in the process of obtaining the ONTV^2 PWM has been the characterization of the output-voltage high-frequency distortion in the 3L-3P NPC dc-ac converter. This need has led to the definition of a novel per switching-cycle figure, $HD_{n,k}$, providing insight into and quantifying the output-voltage distortion around integer multiples of the switching frequency as a function of the modulation pattern selected. We can easily obtain the *THD* of any modulation strategy from the value of this figure over a portion of the line cycle. This figure, applicable to any multilevel converter, significantly simplifies the search of optimum modulation strategies from the point of view of output-voltage high-frequency distortion and is probably the contribution with more potential for a widespread impact of the present thesis.
- The coupling of a conventional control scheme to the proposed modulation can also be accounted as a contribution of the present thesis. In particular, the design of a control loop affecting the modulation pattern to speed-up the recovery from sporadic perturbations in the neutral-point voltage. A complete control has been implemented for a particular application, the connection of a renewable energy source (wind mill, photovoltaic panel,…) to the ac mains with unity power factor and dc-link voltage regulation, proving the goodness of the modulation and control approach developed.
- Overall, a novel methodology to obtain modulation strategies for multilevel three-phase neutral-point-clamped dc-ac converters has been developed. The methodology can be summarized as follows:

    1) Define appropriate virtual space vectors with zero associated average neutral-point currents in each switching cycle.
    2) Generalize the definition of such virtual vectors by allowing any value for the coefficients of the linear combinations defining these virtual vectors.
    3) Formulate an optimization problem with:
        - The design variables being the coefficients of the linear combinations defining the virtual space vectors.
        - The desired objective function to minimize/maximize (typically, a given ac-side three-phase voltage distortion figure.)
        - Appropriate constraints (including the dc-link capacitor voltage balance.)
    4) Solve the optimization problem for all switching cycles within 1/6th of the line cycle to define the optimum modulation strategy.

5) Compute the independent phase duty-ratio from the optimum value of the coefficients found in 4) for all possible modulation index, one line cycle, and all possible ac-side load/source conditions.

6) Approximate the independent phase duty-ratios as a function of the modulation index, line-cycle angle, and ac-side load/source features. It is important to select the most convenient coordinates (e.g., *d-q-0*) to guarantee simple expressions for the phase duty-ratios.

7) Implement the derived modulation with a symmetrical distribution of each phase connection to each of the available dc-link points.

The methodology can also be easily adapted to other types of three-phase dc-ac converters.

These research contributions have already led to the publication of two journal papers [50] [51] and two conference papers [52] [53]. An additional paper proposal for publication in the *IEEE Transactions on Power Electronics* is currently being prepared and two additional conference papers will be submitted, covering the contributions in Chapter 5 and the losses/thermo-dynamical performance comparison among different modulation strategies from Chapters 2 and 4.

6.2. Future Extensions

Among the many possible future extensions of the research reported here, we would like to highlight the following:

- Explore and quantify the advantages in converter size, weight, cost, reliability, and dynamical performance that we can obtain in different practical applications by using the proposed modulation schemes. Study the impact of the different application requirements on the advantage obtained.
- Incorporate the output-voltage high-frequency distortion around twice the switching frequency, three times the switching frequency, etc. (HD_n, $n \geq 2$) in the cost function to minimize, in order to obtain optimum modulation strategies considering a wider spectrum of output voltage distortion.
- Apply the modulation design methodology to other multilevel converters.
- Design the most convenient detection scheme of the non linear-and-balanced nature of the load to activate the non linear-and-balanced load flag employed in the ONTV^2 PWM.

APPENDIX A

EXPERIMENTAL SETUP

Abstract — This appendix contains a description of the experimental setup employed.

A.1. System Overview

Fig. A.1 presents a block diagram describing the overall experimental setup. Three possible sources have been employed: dc power supply, rectified ac mains, and rectified generator voltage. Three loads have been tested: linear *R-L* load, non-linear load, and connection to mains. In the following section, details of the particular components are provided.

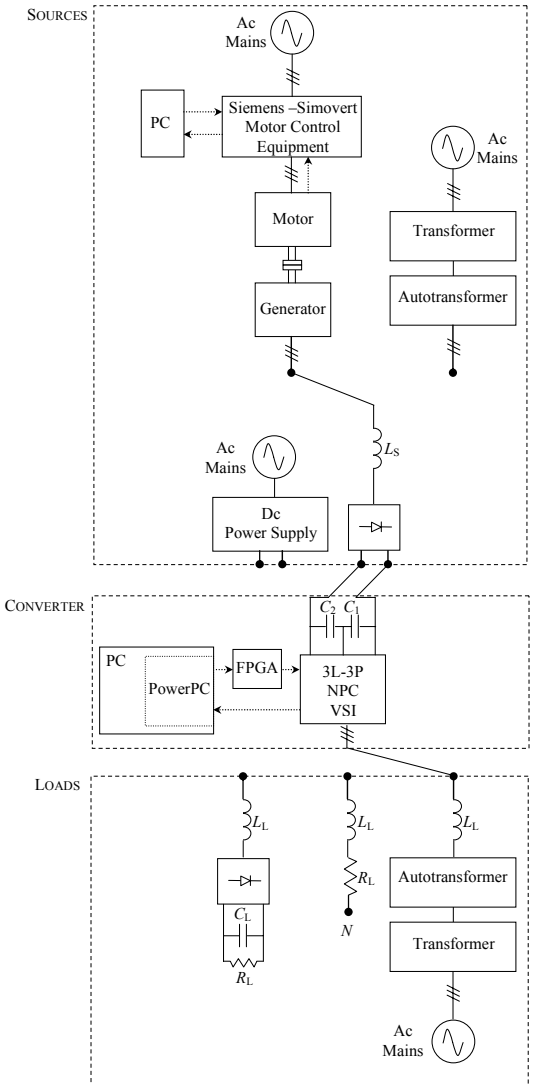


Fig. A.1. Experimental setup diagram.

Fig. A.2. General test bed view.

A.2. Component Details

A.2.1. Sources

A.2.1.1. Dc Power Supply

Fig. A.3. HP 6030A dc power supply.

Maximum dc voltage	200 V
Maximum dc current	17 A
Maximum power	1 kW

Table A.1. Dc power supply specifications.

A.2.1.2. Rectified Ac Mains

Fig. A.4. Transformer – autotransformer set.

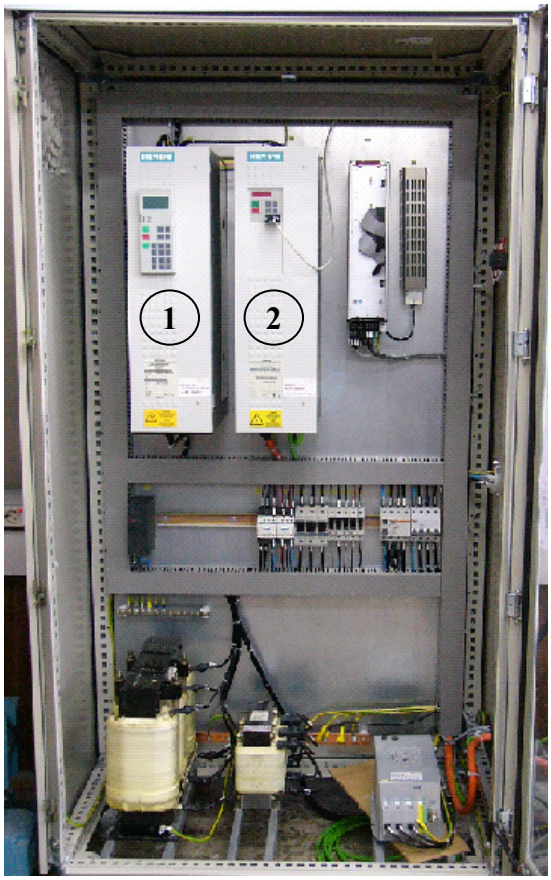
Configuration	3P, Triangle-Triangle
Turns ratio	1:1
Frequency	50 Hz
Nominal line-to-line voltage	380 V_{rms}
Maximum line current	7.6 A_{rms}
Maximum power	5 kVA

Table A.2. Isolation transformer specifications.

Configuration	3P
Frequency	50 Hz
Nominal input line-to-line voltage	400 V_{rms}
Maximum output line-to-line voltage	440 V_{rms}
Maximum input line current	10 A_{rms}
Maximum output line current	10 A_{rms}
Maximum power	7.5 kVA

Table A.3. Autotransformer specifications.

A.2.1.3. Rectified Generator Voltage



1: 37 kW 3P Thyristor Rectifier

2: 37 kW 3P IGBT Inverter

Fig. A.5. Siemens Simovert Masterdrives motor control cabinet.

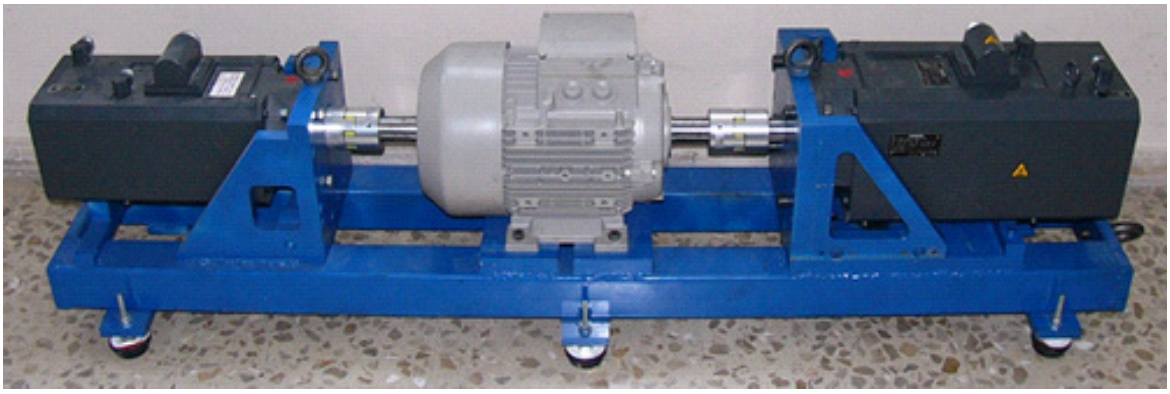


Fig. A.6. Motor-generator set. Motor (left): Siemens 1FT6084-8SH71-1AA0. Generator (right): Siemens 1FT6105-8SB71-2AA0.

Technology	3P synchronous servomotor
Nominal speed	4500 rpm
Maximum speed	7100 rpm
Nominal power	9.4 kW
Nominal torque	20 Nm
Maximum torque @ 0 rpm	26 Nm
Nominal line current	24.5 A
Maximum line current @ 0 rpm	28 A
Nominal line-to-line voltage	261 V_{rms}
Inertia	$4.8 \cdot 10^{-3}$ kgm^2

Table A.4. Motor specifications.

Technology	3P synchronous servomotor
Nominal speed	1500 rpm
Maximum speed	5600 rpm
Nominal power	9.3 kW
Nominal torque	59 Nm
Maximum torque @ 0 rpm	65 Nm
Nominal line current	21.7 A
Maximum line current @ 0 rpm	23.5 A
Nominal line-to-line voltage	284 V_{rms}
Inertia	$16.8 \cdot 10^{-3}$ kgm^2

Table A.5. Generator specifications.

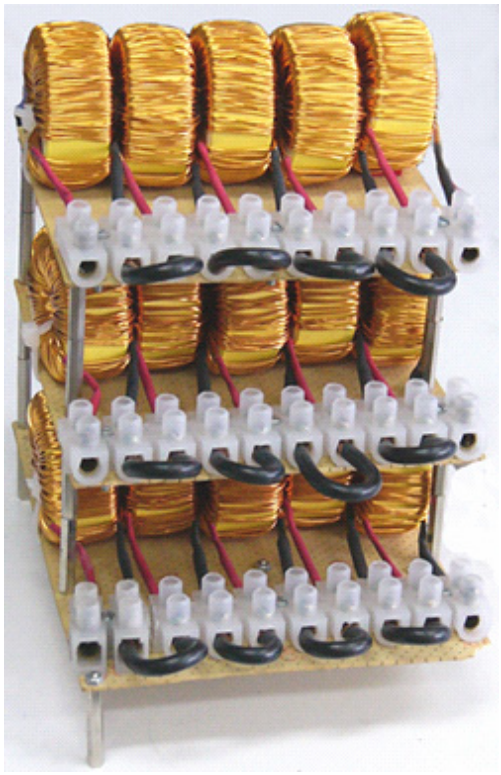


Fig. A.7. Three-phase inductor set.

Core material	Micrometals Iron Powder Mix No. 26
Maximum current	10 A
Average Inductance ([0, 10] A)	2.5 mH
Inductance @ 10A	1 mH

Table A.6. Single toroidal inductor specifications.

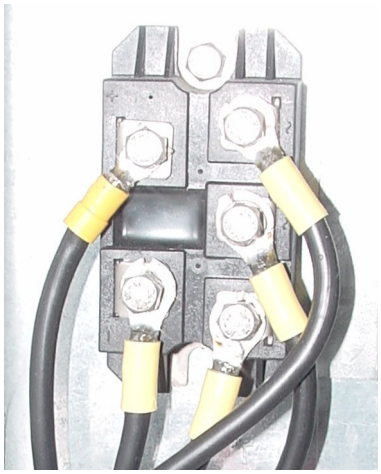
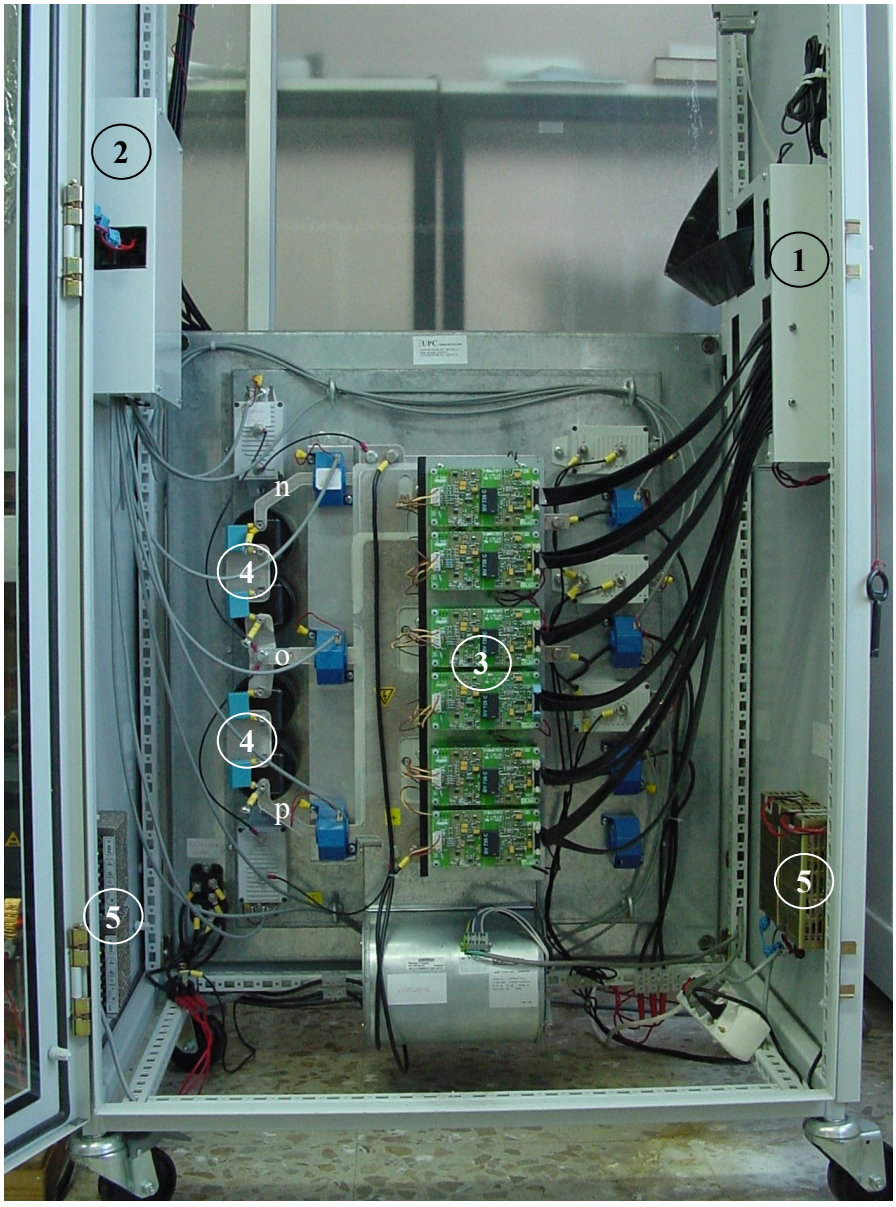


Fig. A.8. DF75AA160 three-phase diode rectifier.

V_{RRM}	1600 V
Maximum output dc current	75 A

Table A.7. Diode module specifications.

A.2.2. Converter



1: Interfacing PowerPC-FPGA-drivers.

2: Analog conditioning of sensor signals.

3: IGBT modules and drivers.

4: Dc-link capacitors.

5: Auxiliary ±15 V dc power supplies.

Fig. A.9. 3L-3P NPC dc-ac converter.

IGBT modules per phase	Semikron SKM 100 GB 123D + SKM 100 GAL 123 D + SKM 100 GAR 123 D
Drivers	Semikron SKHI 10
Dc-link capacitance	$C_1 = C_2 = 1.1$ mF
Maximum dc-link voltage	1500 V
Maximum output line current	180 A_{rms}
Maximum output power	100 kW

Table A.8. Converter specifications.

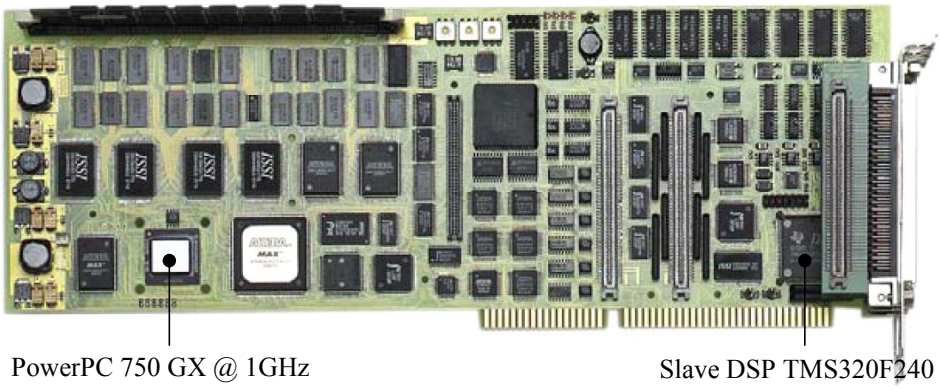


Fig. A.10. dSpace DS1103 PowerPC controller board.

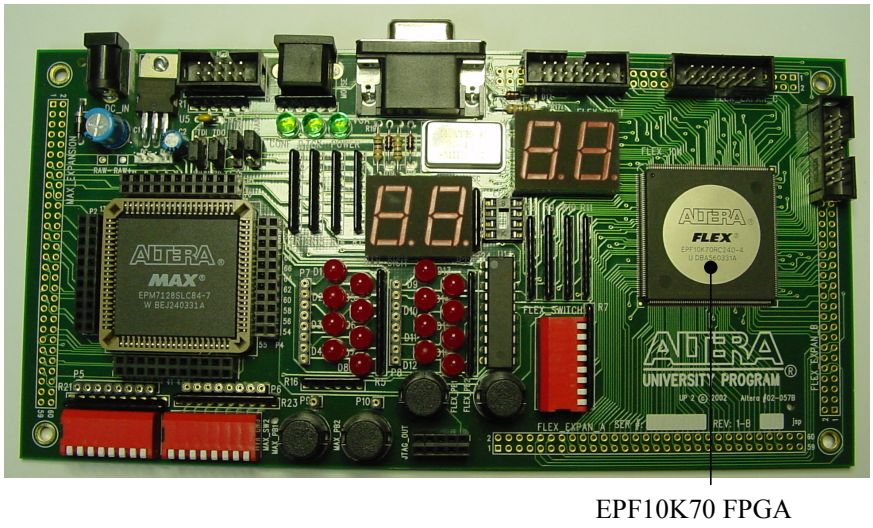
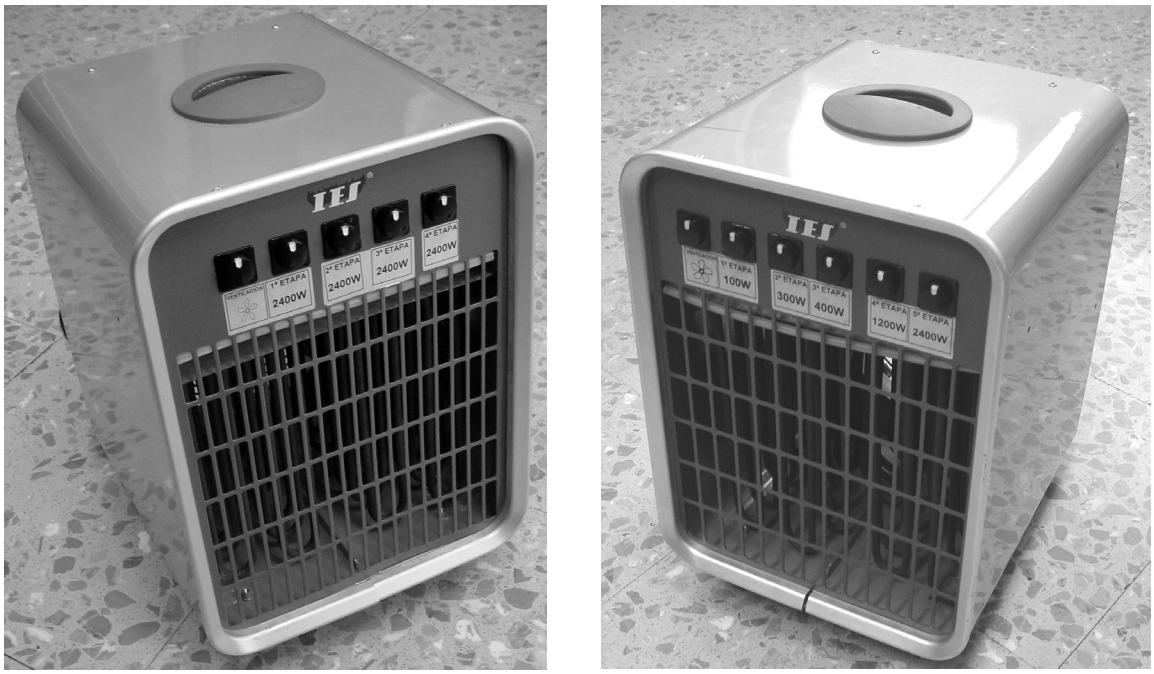


Fig. A.11. Altera University Program board hosting the Altera EPF10K70 FPGA (FLEX10K family).

A.2.3. Loads

A.2.3.1. Linear RL Load

The three-phase inductance set is the same as in Fig. A.7.



(a) *(b)*

Fig. A.12. Three-phase resistive loads. (a) Resistive load 1. (b) Resistive load 2.

Maximum input line-to-line voltage	400 V_{rms}
Selectable resistance per phase	[66, 33, 22, 16.5] Ω
Maximum power	9.6 kW

Table A.9. Resistive load 1 specifications.

Maximum input line-to-line voltage	400 V_{rms}
Selectable resistance per phase	[1587,…, 36] Ω
Maximum power	4.4 kW

Table A.10. Resistive load 2 specifications.

A.2.3.2. Nonlinear Load

The three-phase inductance set is the same as in Fig. A.7.

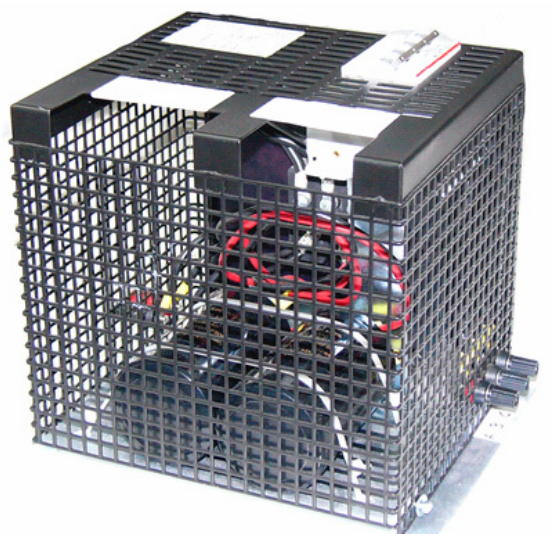


Fig. A.13. Non-linear load module consisting of a three-phase diode rectifier and a capacitor bank.

Capacitance	2 mF
V_{RRM}	400 V
Maximum input line current	14.5 A_{rms}

Table A.11. Non-linear load module specifications.

A.2.3.3. Connection to Mains

The three-phase inductance set is the same as in Fig. A.7. The transformer-autotransformer set is the same as in Fig. A.4.

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